Development of High-Sensitivity Pressure Sensor with On-chip Differential Transistor Amplifier

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Abstract

A mathematical model of a high-sensitivity pressure sensor with a novel electrical circuit utilizing piezosensitive transistor differential amplifier with negative feedback loop (PDA-NFL) is presented. Circuits utilizing differential transistor amplifiers based on vertical n-p-n and lateral p-n-p transistors are analyzed and optimized for sensitivity to pressure and stability of output signal in operating temperature range. Parameters of fabrication process necessary for modeling of I-V characteristics of transistors are discussed. The results of the model are sufficiently close to the experimental data.

Keywords: bipolar junction transistor, sensor model analysis, piezosensitivity, pressure sensors, stability

1. Introduction

One of the key events that opened road for development of piezoresistive sensors was invention of piezoresistive effect in silicon and germanium by Smith C.S. in 1954 [1]. Piezoresistive effect was used in development of pressure and force sensors as well as accelerometers. Today piezoresistive pressure sensors are dominating in the pressure sens-ing market and attracting a lot of R&D resources. The most significant event in microelectronics was invention of tran-sistor in December 1947 by Brattain W.H. and Bardeen J. with contribution of Shockley W.B. [2]. Little bit later transistor has been independently described by Krasilov A.B. and Madoyan C.G. in [3]. First studies of piezoeffect in BJT performed in 1960-70s by W. Rindner, R. Edwards, Y. Kanda, M.E. Sikorski and A.L. Polyakova [4-8] were not related to development of pressure sensors. Piezoeffect was evaluated based on modulation of I-V curves of Si and Ge transistors by pressure applied with help of a needle. In these tests, mechanical stress could be as high as 1 GPa. In mid 1970s, use of bipolar junction transistor (BJT) in pressure sensor chips was proposed by V.I. Vaganov [12]. The first detailed paper on pressure sensor utilizing BJT was published by V.I. Vaganov in [9]. Later, the topic was discussed in a book [10], patents [11-13] and in a recent publication [14]. The results reported by Vaganov et al. are in good agreement with publication by Fruett F. and Meijer G.C.M. (Delft University of Technology), who described stress-sensitive behavior of elements with p-n junctions and called it “piezojunction effect” [15]. It is worth mentioning that initially the authors did not have an intention to develop a stress sensor. They studied parasitic effects in temperature sensors caused by mechanical stress.

Use of BJTs either as stress-sensitive components or as elements of stress-sensitive circuits is a promising direction in development of MEMS pressure sensors. This approach allows for increase of pressure sensitivity compared to pressure sensors utilizing Wheatstone bridge circuit formed by piezoresistors while keeping the same size of the diaphragm and power supply. Alternatively, it can be used to reduce size and cost of pressure sensor die and/or increase its overload capability without reducing sensitivity to pressure. The last task is typically solved by changing geometry of diaphragm [16-29].

Main drawbacks of circuits based on BJTs are strong temperature dependence of output signal and higher noise compared to traditional piezoresistive pressure sensors [30-32]. This paper discusses method of decreasing high temperature dependence of output signal and increasing pressure sensitivity of sensor by using novel piezosensitive transistor differential amplifier (PDA) circuits utilizing vertical npn BJTs (V-NPN) and horizontal pnp BJTs (L-PNP) and using negative feedback loop (NFL). Fabrication process and parameters important for modeling of I-V characteristics of transistors and options for noise reduction are also discussed.

2. Methods

1.1 Analysis and modelling of Electrical circuit

The piezosensitive transistor differential amplifier with negative feedback loop (PDA-NFL) circuit was analyzed using an analytical mathematical model and modeled with help of NI Multisim software. Two circuits utilizing V-NPN and L-PNP BJTs are shown in Figure 1.

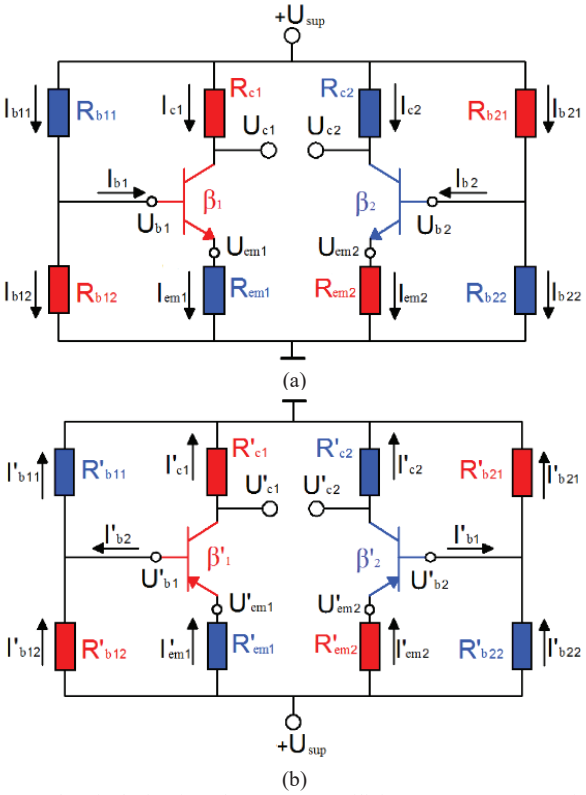


Fig. 1. Electrical circuits of PDA-NFL utilizing: (a) V-NPN transistors; (b) L-PNP transistors.

Resistors increasing their values and transistors increasing gain β when pressure is applied are highlighted by red color, resistors decreasing their values and transistors decreasing gain β when pressure is applied are highlighted by blue color. Analysis is performed under an assumption that pressure is applied on the back side of the diaphragm. To simplify the analysis, let us use the fact that circuits are symmetrical and consider one side of the differential amplifier. When pressure is applied, then components on the other side of the circuit change in a reverse direction forming signal having reverse polarity. Therefore, differential output signal of PDA circuit is twice bigger than the signal generated by one side of the circuit. Main equations used in the analysis of V-NPN transistor circuit parameters are provided below. Apostrophe (') is added to the variables in equations for circuit utilizing L-PNP transistors.

$$I_{c1} = \beta_1 \cdot I_{b1}, \tag{1}$$

$$I_{em1} = (\beta_1 + 1) \cdot I_{b1}, \tag{2}$$

$$\theta = (R_{b11} + R_{b12}) / R_{b12}, \tag{3}$$

$$I_{b1} = [U_{sup} - \theta \cdot (U_{b1} - U_{em1})] / [R_{b11} + \theta \cdot (1 + \beta_1) \cdot R_{em1}], \tag{4}$$

$$I_{b11} = (U_{sup} + I_{b1} \cdot R_{b12}) / (R_{b11} + R_{b12}), \tag{5}$$

$$I_{b12} = (U_{sup} - I_{b1} \cdot R_{b1}) / (R_{b11} + R_{b12}), \tag{6}$$

$$U_{sup} = I_{b11} \cdot R_{b11} + I_{b12} \cdot R_{b12}, \tag{7}$$

$$U_{b1} = (I_{b11} - I_{b1}) \cdot R_{b12}, \tag{8}$$

$$U_c = U_{sup} - \beta_1 \cdot I_{b1} \cdot R_{c1}, \tag{9}$$

$$U_{em1} = U_{sup} - \theta \cdot (U_{b1} - U_{em1}) / [\theta + R_{b11} / ((\beta_1 + 1) \cdot R_{em1})], \tag{10}$$

Equation (1) – (10) describe currents and voltages in the circuit utilizing V-NPN transistors. U_{sup} – supply voltage – 5.00 V supply voltage was used in the circuit analysis; $U_{b1,\ c1,\ em1}$, $I_{b1,\ c1,\ em1}$ – base, collector and emitter potentials and currents of V-NPN transistor, correspondingly; β_1 – current gain coefficient; $R_{b11,\ b12}$ and $I_{b11,\ b12}$ – resistors forming divider defining base potential and currents in the divider; R_{c1}, R_{em1}– resistance of collector and emitter resistors, θ – dimensionless parameter used in some equations. The equations are derived under assumption that resistance of transistor base is significantly lower compared to resistance of resistors R_{b11} and R_{b12} forming base divider. It is necessary to take into account parasitic component of emitter current flowing vertically through the base to the substrate. Epitaxial wafers with n-type epi-layer grown on top of p-substrate can be used to make the described circuits. Isolation of vertical transistors from each other can be achieved by diffused isolating areas having p-type conductivity and extending through the full thickness of the epi-layer. It is worth mentioning that L-PNP transistor can be formed on standard p-type Si wafers within n-doped pockets. The parasitic component of emitter current has been evaluated with help of Sentaurus TCAD software. Data on doping of layers used to form L-PNP transistors (and resistors) are presented (Figure 2(a)) to allow for more

detailed analysis of the parasitic component of emitter current in L-PNP transistor with one collector area. As it can be seen from Figure 2(b), parasitic component k of L-PNP transistor as the ratio of emitter current flowing into the substrate to total emitter current decreases from 65% to 50% when base current increases from 0.05 mA to 1.00 mA (black line – emitter current, blue line – parasitic current, green line – parasitic component k).

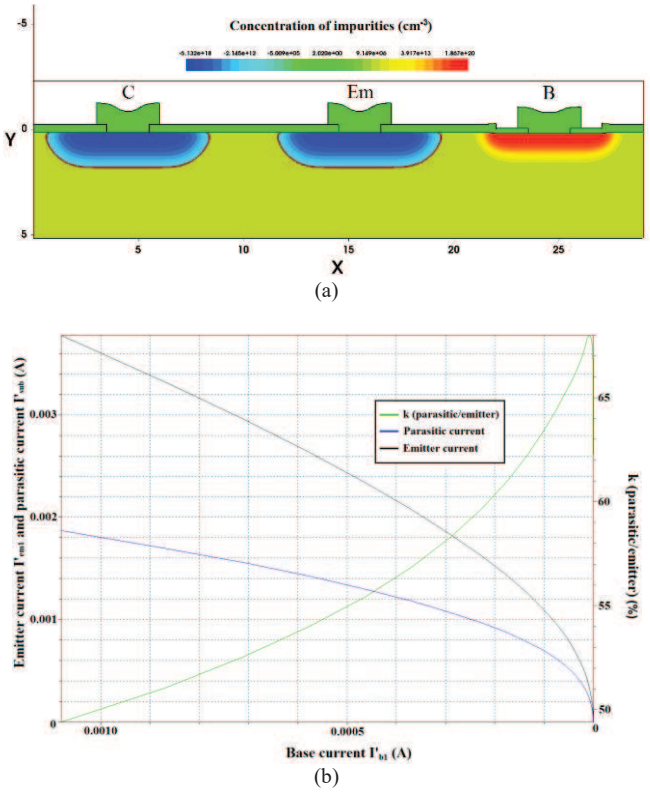


Fig. 2. Results of analysis of L-PNP transistor in TCAD: (a) structure of the transistor with doping map; (b) I-V characteristic for dependence of emitter and parasitic current on base current and analysis of parasitic component of emitter current flowing to the substrate on base current.

Therefore, it is necessary to modify equations (1-10) for L-PNP transistor and take into account this parasitic component in the equations for emitter current and emitter voltage:

$$I'_{em1} = I'_{em1u} + I'_{sub}, \quad (11)$$

$$U'_{em1} = (I_{em1u} + I'_{sub}) \cdot R'_{em1}, \quad (12)$$

where I'_{em1} – emitter current of L-PNP transistor having two components: I'_{em1u} – "useful" emitter current and I'_{sub} – parasitic current flowing to the substrate of L-PNP transistor, U'_{em1} – emitter potential with respect to ground, R'_{em1} – resistance of emitter resistors L-PNP transistor. It is possible to minimize or even eliminate the parasitic current by using diaphragm thickness equal or somewhat smaller than thickness of epi-wafer. Alternatively, SOI wafers with thin device layer also can be used as starting material. In that case, diffusion through the device layer can be used to form collector surrounding emitter area. It also will minimize the parasitic current.

1.2 Stress sensitivity

All components of the electrical circuit (8 resistors and 2 transistors) are located in diaphragm areas with maximum values of mechanical stress. No topological limitations on placement of different components on the diaphragm are taken into account in the analysis. Relationships between mechanical stress and corresponding change of resistance in piezoresistors and change of gain coefficient β in the transistors are taken from theory of piezoresistive and piezojunction effects. As a first step, analysis of maximum stress in the pressure sensing element having diaphragm with three rigid islands will be performed. Geometry of sensing element is shown in Figure 3.

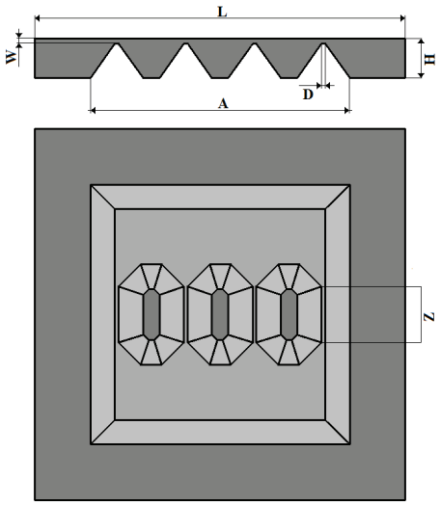


Fig. 3. Structure of pressure sensing element.

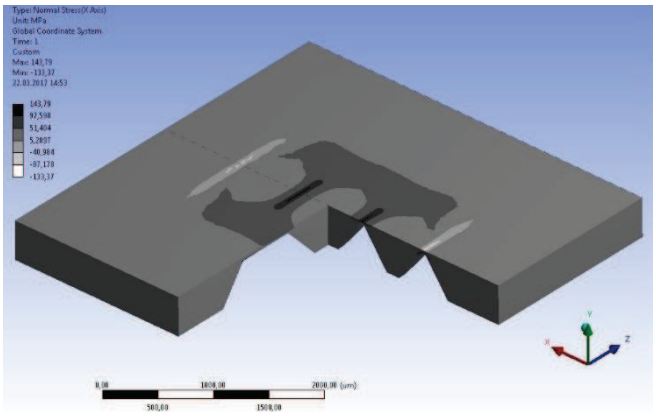
Table 1 provides information about geometrical parameters of pressure sensing element: L – side length of the die (die is square), W – diaphragm thickness, H – wafer thickness, A – diaphragm length (diaphragm is square), D – target width of grooves between rigid islands and between rigid islands and the frame, Z – target edge length of the rigid island.

Table 1. Main geometrical parameters of the sensing element.

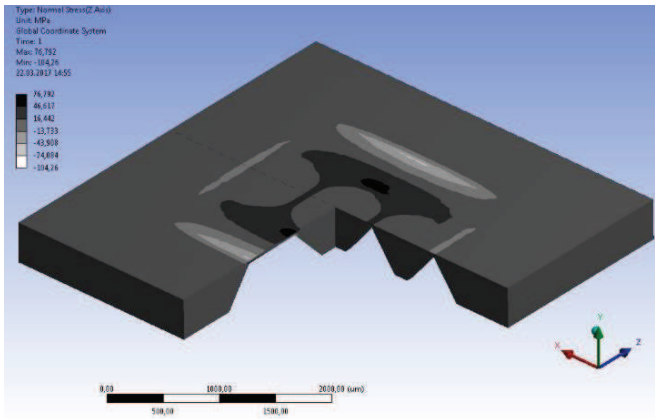
Geometrical Parameter	Size, μm
L	4000
W	33
H	420
A	2810
D	41
Z	490

Stress distribution in the sensing element was obtained using FEA modeling in ANSYS for transverse (Figure 4(a)) and longitudinal (Figure 4(b)) mechanical stress of piezoresistors figure. Brick-shaped elements having size of 50 μm were used in bulk areas. Areas where circuit components are located used finer meshing – 15 μm elements.

Table 2 provides parameters of piezoresistive and piezojunction effects. Piezoresistive coefficient π_{44} is calculated using equations from [33] for surface concentration of $N_S = 6 \cdot 10^{18}$ cm^{-3} (corresponding sheet resistance is 200 Ohm/cm^2 and depth of p-n junction x_j = 2.2 μm). Averaged values of piezojunction coefficients (ξ_{44} V-NPN и ξ_{44} L-PNP) taken from [34-36] and corresponding to target process parameters were used in the model. Figure 4 shows two stress components in plane of the diaphragm: σ_Z and σ_X – parallel and perpendicular to the longitudinal axes of the grooves when the diaphragm is loaded by pressure ΔP = 100 kPa.



(a)



(b)

Fig. 4. The distribution of the mechanical stress in the sensing element: (a) transverse, along the X axis; (b) longitudinal, along the Z axis.

Change of resistance of piezoresistors can be calculated using equation:

$$\Delta R_i(P) = (dR_i(P)) \cdot R_i = R_i \cdot (\pi_{44} / 2) \cdot \sigma_j, \qquad (13)$$

where $\Delta R_i(P)$ – change of resistance of resistor R_i, $dR_i(P)$ – relative change of resistance of resistor R_i, σ_j – stress in the area where resistor R_i is located. The equation is valid for all resistors in the circuit. It needs to be taken into account that resistors R_{b12}, R_{c1}, R_{em2}, R_{b21}, R'_{b12}, R'_{c1}, R'_{em2}, R'_{b21} are located in the areas with compressive stress, while resistors R_{b11}, R_{em1}, R_{c2}, R_{b22}, R'_{b11}, R'_{em1}, R'_{c2}, and R'_{b22} – in the areas with tensile stress.

Table 2. Parameters of piezoresistive and piezojunction effects.

Parameters		Values: Compressive stress	Values: Tensile stress	Units
Mechanical stress	Longitudinal, Z, $\sigma_{i\,Z}$	111	-111	MPa
	Transverse, X, $\sigma_{i\,X}$	34	-30	
	Total, σ_i	77	-81	
Piezoresistive coefficient, π_{44}		126.0		10^{-11}·Pa^{-1}
Piezojunction coefficients	$\xi_{44\,V\text{-}NPN}$	13.1		
	$\xi_{44\,L\text{-}PNP}$	111.2		

Change of transistor gain can be calculated using equation:

$$\Delta\beta_k(P) = (d\beta_k(P)) \cdot \beta_k = \beta_k \cdot (\xi_{44} / 2) \cdot \sigma_j, \qquad (14)$$

where $\Delta\beta_k(P)$ – change of gain β_k of transistor k, $d\beta_k(P)$ – relative change of gain β_k of transistor k. Transistors having gain β_1 и β'_1 located in the areas with compressive stress, while transistors having gain β_2 и β'_2 located in the areas with tensile stress. To find change of collector potential for one of transistors, it is convenient to use equation (9) and take into account induced by stress change of resistance of piezoresistors and change of transistor gain defined by (13, 14). Full output signal ΔU(P) is equal to the difference between potentials $\Delta U_{c1}(P)$ и $\Delta U_{c2}(P)$:

$$\Delta U(P) = \Delta U_{c1}(P) - \Delta U_{c2}(P), \qquad (15)$$

Final value of circuit sensitivity S can be presented as:

$$S = \Delta U(P) / (U_{sup} \cdot \Delta P), \qquad (16)$$

where ΔP – nominal pressure.

1.3 Temperature stability

Analysis of temperature stability of PDA-NFL electrical circuit utilizing V-NPN transistors can be performed using the following equations [37]. Apostrophe (') is added to the variables in equations for circuit utilizing L-PNP transistors:

$$\gamma = [\beta_1 \cdot (1 + R_{em1} \cdot \theta)]/(\beta_1 \cdot R_{em1} \cdot \theta / R_{b11} + 1), \quad (17)$$

$$R_{b11} = [(\gamma - 1) \cdot U_{sup} \cdot R_{em1}]/[R_{em1} \cdot I_{em1} + (U_{b1} - U_{em1})], \quad (18)$$

$$R_{b12} = R_{b11}/[U_{sup}/(R_{em1} \cdot I_{em1} + (U_{b11} - U_{em1})) - 1), \quad (19)$$

$$R_{c1} = (U_{sup} - U_{c1})/I_{c1}, \quad (20)$$

$$R_{em1} = [U_{c1} - (U_{c1} - U_{b1}) - (U_{b1} - U_{em1})]/I_{em1}, \quad (21)$$

where γ – parameter defining level of stability of circuit parameters over temperature range. Parameter γ changing from 1.5 to 4.0 depending on required ratio of useful output signal (sensitivity) and its stability over temperature range. Equations (18-19) are derived using (17). Only one half of the differential circuit is analyzed to simplify the task. Despite the symmetry of PDA-NFL circuit, change of output signal with temperature strongly affected by dependence of collector potential $\Delta U_{ci}(T)$, i = 1.2 in both halves of the non-ideal circuit having differences between circuit elements caused by process variations. Parameter TCZ can be used to calculate temperature dependence of output signal at zero pressure. Analysis of temperature stability was performed for typical values of temperature coefficient of base-emitter voltage $\Delta(U_{b1}\text{-}U_{em1})(T)/T \approx$ -2.0 mV/^{0}C, resistance of piezoresistors TCR ≈ 0.12 %/^{0}C and gain TCβ ≈ 0.8 %/^{0}C. TCZ shows change of circuit output signal per one degree Centigrade as a percentage of span and measured in %FS/ºC:

$$TCZ = [U_{c1}(T_1) - (U_{c1}(T_{room})]/ [\Delta U(P) \cdot (T_1 - T_{room})] \cdot 100\%, \quad (22)$$

where $U_{c1}(T_{1,\,room})$ – output signal of one side of PDA-NFL electrical circuit at temperatures T_1 and T_{room}, correspondingly. Importance of parameter TCZ is related to its link to sensor sensitivity and span. Therefore, it allows for evaluation of impact of temperature error on sensor accuracy.

2. Results

2.1 Extraction of circuit parameters

It is necessary to define some input parameters for analysis of bipolar junction transistors. Two types of BJTs are selected for analysis not only because of difference in piezojunction coefficients but also because of difference in the structure of these transistors resulting in relatively high gain $\beta_{1,2}$ of V-NPN transistor and relatively low gain $\beta'_{1,2}$ of L-PNP transistor. As limit cases in the study, average gain of V-NPN transistor is assumed to be $\beta_{1,2}$ = 150 while gain of L-PNP transistor is chosen to be $\beta'_{1,2}$ = 5. Following I-V curve was calculated for pre-selected geometry and dopant concentration of BJTs shown in Figure 5 and process described in Table 3.

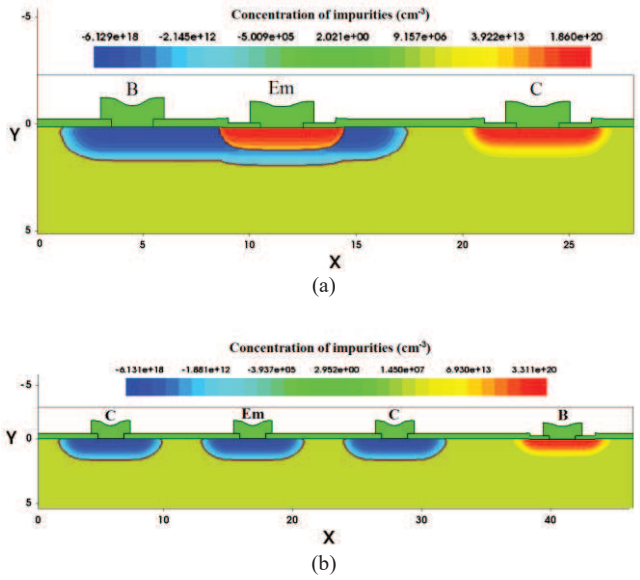


Fig. 5. Geometry and dopant concentration of transistors for: (a) V-NPN transistor; (b) L-PNP transistor.

V-NPN и L-PNP transistors are created in the same process and transistor depth was assumed to be equal to 10 μm. High target value of gain coefficient β of V-NPN transistor and using two collector areas in L-PNP transistor has been chosen also to minimize noise component of output signal. Due to thinner base layer in V-NPN transistor and increased perimeter to area ratio of the active base area for L-PNP transistor current gain β will increase, but flicker noise and thermal noise will drop, due to smaller resistance of transistor base [38].

Table 3. Fabrication process.

Process step	Parameters
Oxidation	1100 ºC, 15 min.-20 min.-15 min (dry-wet-dry)
Isolation diffusion of boron to separate transistors in epitaxial layer	Diffusion from unlimited source: 1050 ºC, 55 min. Drive-in: 1200 ºC, 330 min.
Forming high-doped P+ areas	Diffusion from unlimited source: 1050 ºC, 55 min. Drive-in and oxidation: 1150 ºC, 5 min – 15 min. – 5 min (dry-wet-dry)
Forming P-resistors, base of V-NPN transistor, collector and emitter areas of L-PNP transistor	Ion implantation: D = $8.0 \cdot 10^{14}$ cm^{-2}, E = 50 keV Impurity activation and oxidation: 1100 ºC for 45 min in inert atmosphere followed by oxidation 1000 ºC, 5 min – 35 min. – 5 min. (dry-wet-dry)
Forming N- base of L-PNP transistor, collector and emitter of V-NPN transistor	Ion implantation: D = $10.4 \cdot 10^{15}$ cm^{-2}, E = 70 keV Impurity activation and oxidation: 1030 ºC, 25 min. in inert atmosphere followed by oxidation 1030 ºC, 5 min – 35 min. – 5 min. (dry-wet-dry)

Base currents $I_{B1,2}$ or $I'_{B1,2}$ are evaluated from I-V curves obtained in Sentaurus TCAD. Figure 6(a) shows dependence

of gain $\beta_{1,2}$ on collector current $I_{c1,2}$ for V-NPN transistor. Figure 6(b) shows dependence of gain $\beta'_{1,2}$ on collector current $I'_{c1,2}$ for L-PNP transistor.

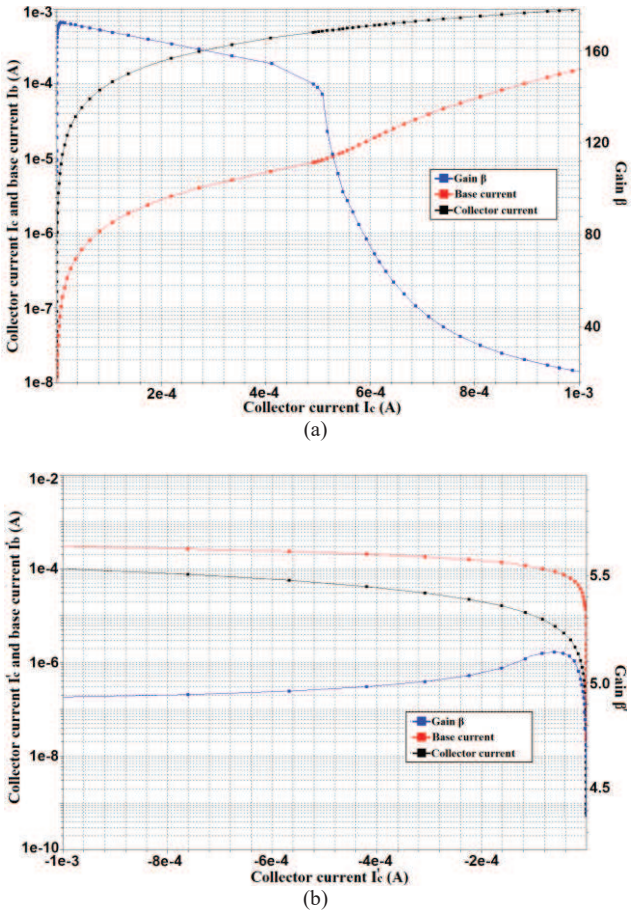


Fig. 6. Dependence of gain β on collector current: (a) V-NPN transistor; (b) L-PNP transistor.

As it can be seen from the graphs, there are ranges of base current where gain β has weak dependence on collector current. It makes sense to use these ranges when selecting work point of the circuit. Therefore, in the further analysis it will be assumed that base current of V-NPN transistor is equal to $I_{b1,2} = 5$ μA and for base current for L-PNP transistor is equal to $I'_{b1,2} = 50$ μA. Corresponding voltage drop at base-emitter junction is equal to $(U_{b1}\text{-}U_{em1}) = 0.80$ V for V-NPN and $(U'_{b1}\text{-}U'_{em1}) = 0.78$ V for L-PNP transistors. An additional requirement to circuits with differential transistor amplifiers is getting potentials of differential outputs approximately at one half of voltage supply at ΔP = 0 kPa and T = 300 K:

$$U_{c1,2} = U'_{c1,2} \approx U_{sup} / 2, \qquad (23)$$

This condition should be met to enable subsequent analog or digital processing of output signal by ASIC. Evaluated analytically circuit parameters were verified using NI Multisim software. Let us analyze temperature dependence of output signal, sensitivity and other parameters as a function of parameter γ. If parameter γ changes, then five parameters in (18-21) that determine values of four resistors R_{b11}, R_{b12}, R_{c1}, R_{em1} or R'_{b11}, R'_{b12}, R'_{c1}, R'_{em1} and voltage drop between collector and base of transistors $(U_{c1}\text{-}U_{b1})$ or $(U'_{c1}\text{-}U'_{b1})$ for V-NPN и L-PNP transistors, correspondingly, also change their values. At the next step, let us define voltage drop between collector and base from equation (21). Voltage drop $(U_{c1}\text{-}U_{b1})$ and $(U'_{c1}\text{-}U'_{b1})$ should be higher than 0 V and lower than $(U_{c1}\text{-}(U_{b1}\text{-}U_{em1})\text{-}I_{em1}\cdot R_{em1})$ or $(U'_{c1}\text{-}(U'_{b1}\text{-}U'_{em1})\text{-}I'_{em1}\cdot R'_{em1})$. If $(U_{c1}\text{-}U_{b1})$ is close to 0 or $(U'_{c1}\text{-}U'_{b1})$ is close to 0, then transistor is not fully in active regime. If $(U_{c1}\text{-}U_{b1})$ or $(U'_{c1}\text{-}U'_{b1})$ is close to maximum, then at any value of parameter γ in the range of 1.5 to 4.0 resistance R_{b2} is smaller than 400 Ohm. However, at used sheet resistance of $R_S = 200$ Ohm/cm^2, process variability caused by variation of doping level and side diffusion of impurity will result in a wide distribution of circuit offset. Therefore, the following assumption was made: voltage drop both on collector-base junction $(U_{c1}\text{-}U_{b1})$ or $(U'_{c1}\text{-}U'_{b1})$ and on emitter resistors $I_{em1}\cdot R_{em1}$ or $I'_{em1}\cdot R'_{em1}$ are close to each other and close to one half of possible range and close to 0.85 V. This assumption allows for reaching balance of circuit parameters. Under this assumption, increasing parameter γ will cause increase of resistors R_{b11}, R_{b12} or R'_{b11}, R'_{b12}, which form base voltage divider and decrease both piezosensitivity $S_{V\text{-}NPN}$ or $S_{L\text{-}PNP}$ and temperature error $TCZ_{V\text{-}NPN}$ or $TCZ_{L\text{-}PNP}$ for PDA-NFL electrical circuits utilizing V-NPN and L-PNP transistors, correspondingly. All these parameters change almost linearly. It is important to consider a restriction on values of resistors R_{b11}, R_{b12} and R'_{b11}, R'_{b12}. Their values should be in the range of 1.0 to 10.0 kOhm due to both space limitations in the area where resistors should be placed and sheet resistance of the layer used to form these resistors. As sheet resistance is close to 200 Ohm/cm^2, it makes sense to use resistor having at least 5 squares to minimize difference between resistors due to process variations. Adding trimmable resistors located on the frame of the chip to PDA-NFL circuit can be a promising option to enhance chip design. These resistors can be non-sensitive to pressure and allow for accurate balancing of the circuit. After parameters I_b, β, $(U_c\text{-}U_b)$, $(U_b\text{-}U_{em})$ and U_c are determined analysis for balance between temperature stability and sensitivity showed that optimum values of parameter γ can be: $\gamma_{V\text{-}NPN} = 2.00$ for the circuit based on V-NPN transistors and $\gamma_{V\text{-}NPN} = 1.25$ – L-PNP transistors.

NI Multisim software was used for a detailed analysis of circuit parameters. The circuit was modeled by combining discrete elements with predetermined parameters. Gummel-Poon model was used for BJT description. Reverse current of collector junction was calculated based on analysis of a stand-alone transistor with a requirement of getting base current of $I_b = 0.3$ μA at a given emitter-base voltage $U_b\text{-}U_{em}$. Figure 7 summarizes modeling results for electrical circuit

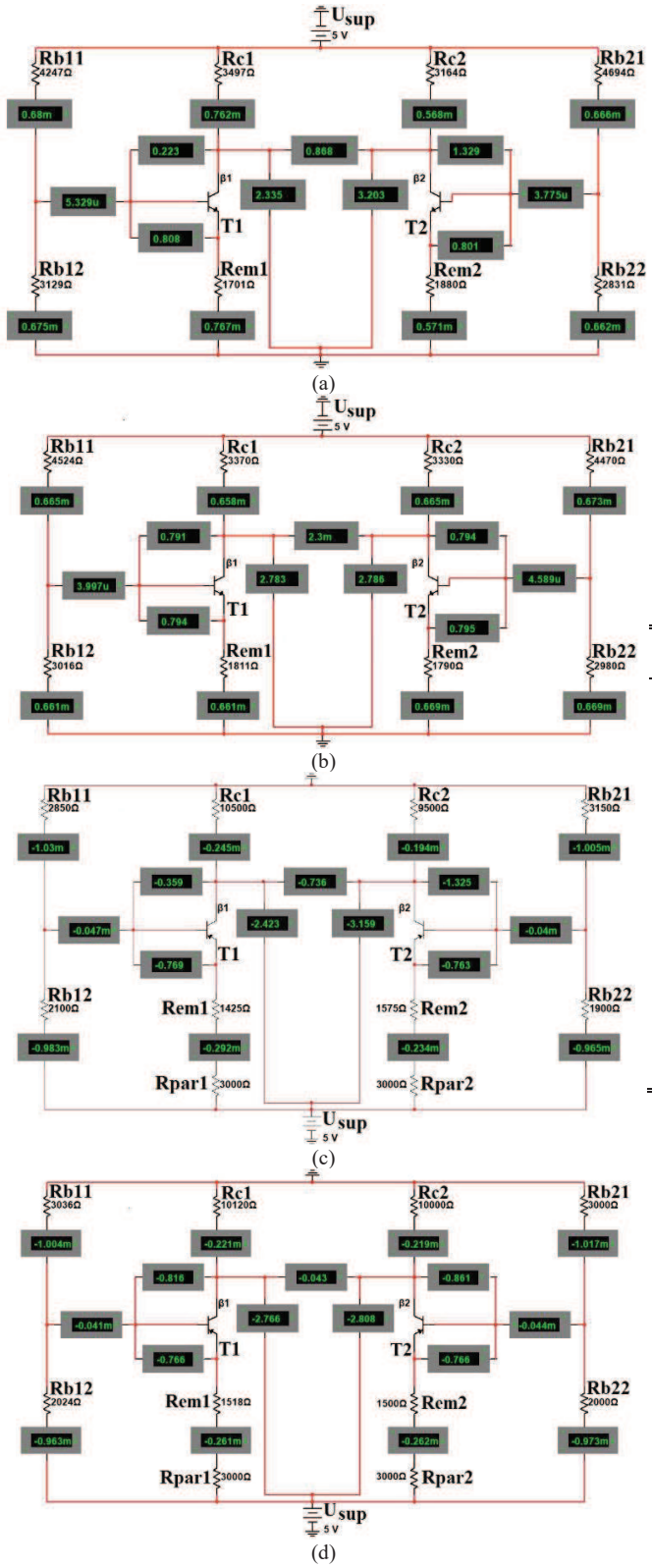


Fig. 7. Parameters of PDA-NFL circuits calculated in NI Multisim: circuit based on V-NPN transistors loaded by pressure (a) and temperature (b); circuit based on L-PNP transistors loaded by pressure (c) and temperature (d).

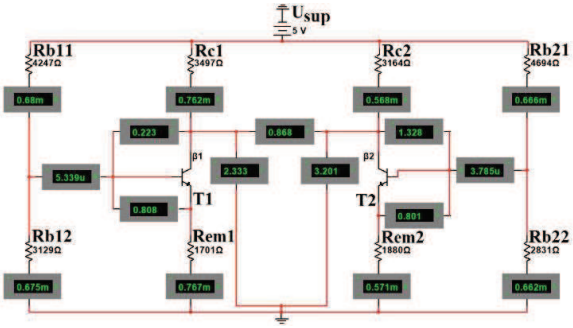
when sensor chip is loaded by ΔP = 100 kPa pressure (a, c) and temperature ΔT = 10 ^{0}C (b, d). To illustrate temperature dependence of circuit parameters, left side of the circuit is shown with parameters affected by temperature increase by 10 ^{0}C (T_1 = 37 ^{0}C) while the right side shows circuit parameters at temperature T_{room} = 27 ^{0}C. As it can be seen from values shown in the right side of the circuits based on V-NPN and L-PNP transistors in Figure 7 (b, d), modeling results are close to circuit parameters calculated analytically.

In case of circuit based on L-PNP transistors it is necessary to take into account parasitic current flowing from emitter to substrate. At $I'_{b1,2}$ = 50 μA the parasitic current accounts for about 67 % of total emitter current. Effect of the parasitic current can be represented in PDA-NFL electrical circuit by a resistor connected in series with R'_{par} and equal to 3.0 kOhm. Table 4 shows all parameters recommended for PDA-NFL circuits. Apostrophe (') is added to the variables in equations for circuit utilizing L-PNP transistors.

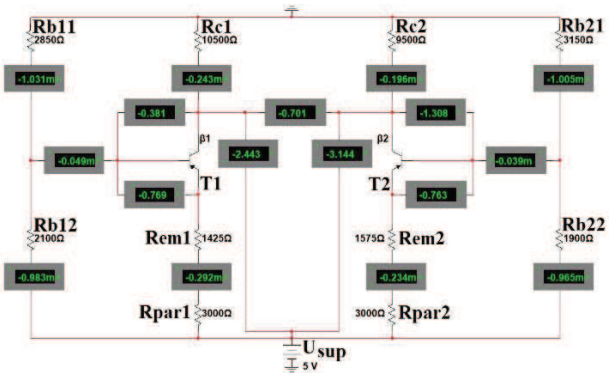
Table 4. Parameters of PDA-NFL circuit.

Parameters	V-NPN circuit		L-PNP circuit	
	Analytical	Multisim	Analytical	Multisim
Base current BJT I_b, μA	5.0	4.6	50.0	44.0
Gain BJT β	150	145	5	5
Base-emitter voltage drop BJT ($U_b - U_{em}$), V	0.80	0.80	0.78	0.77
Collector-base voltage drop BJT ($U_c - U_b$), V	0.85	0.80	0.86	0.86
Collector potential BJT U_c, V	2.50	2.79	2.50	2.81
Parasitic current to substrate BJT I_{par}, μA	-		33.0	
$R_{b11, B21}$, kOhm	4.47		3.00	
$R_{b12, B22}$, kOhm	2.98		2.00	
$R_{c1, c2}$, kOhm	3.33		10.00	
$R_{em1, em2}$, kOhm (without parasitic substrate current)	1.79		4.50	
$R_{em1, em2}$, kOhm (with parasitic substrate current)	-		1.50	
Parameter γ	2.00		1.25	

A version of the circuit with transistors not sensitive to applied pressure was analyzed to evaluate contribution of transistors to overall pressure sensitivity. Results are presented in Figure 8. This version can be implemented by placing transistors on the frame. It allows for achieving more symmetrical layout of components and avoiding connections between active and passive components on the diaphragm.



(a)

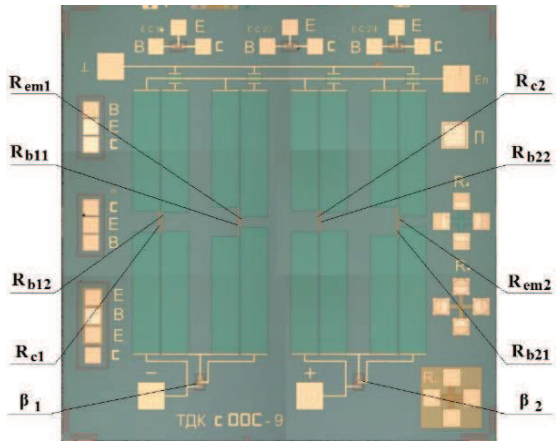


(b)

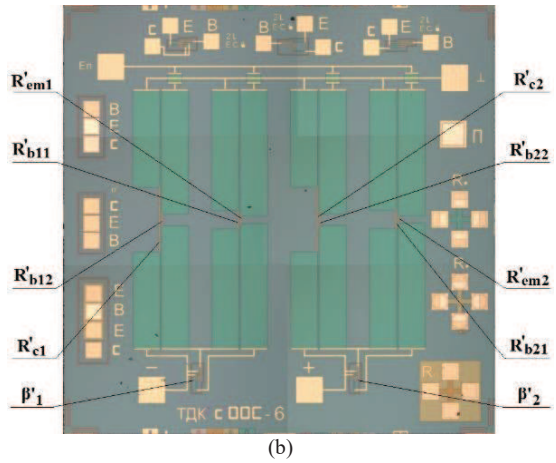
Fig. 8. Values of electrical circuit components for PDA-NFL chip loaded by pressure (transistor not loaded by mechanical stress) from NI Multisim software: (a) circuit on V-NPN transistors; (b) circuit on L-PNP transistors.

2.2 Measurements of experimental samples

Sensor chip with PDA-NFL circuit utilizing V-NPN transistors is shown in Figure 9(a) and sensor chip with circuit utilizing L-PNP transistors is shown in Figure 9(b).



(a)



(b)

Fig. 9. Sensor chip with PDA-NFL circuit: a) top view of chip with V-NPN BJT circuit, b) top view of chip with L-PNP BJT circuit.

Transistors are non-sensitive to pressure. Table 5 provides experimental and theoretical (in brackets) values of performance parameters for pressure sensor utilizing PDA-NFL circuit and for pressure sensor (TM) utilizing classic Wheatstone bridge (with identical chip geometry) formed by four piezoresistors and powered by constant voltage of 5.0 V and for the differential pressure range of 60 kPa.

Table 5. Parameters of pressure sensor chip with PDA-NFL circuit and TM.

Parameter	Sensor Chip		
	PDA-NFL with V-NPN	PDA-NFL with L-PNP	TM
Sensitivity S (model), mV/V/kPa	1.877 (1.740)	1.216 (1.400)	0.515 (0.500)
Zero pressure output signal (Offset), mV/V	6.8	9.2	3.0
Noise voltage, μV/V	3	12	0.8
Nonlinearity $2K_{NL}$, %FS	0.059	0.051	0.055
TCZ (–30…+20 °C) (model), %FS/°C	0.007 (0.026)	0.051 (0.584)	0.003
TCZ (+20…+60 °C) (model), %FS/°C	0.010 (0.026)	0.056 (0.584)	0.002
TCS (–30…+20 °C), %FS/°C	0.020	0.005	0.043
TCS (+20…+60 °C), %FS/°C	0.045	0.011	0.034
Zero thermal hysteresis (–30…+20°C), %FS	0.065	0.252	0.033
Zero thermal hysteresis (+20…+60°C), %FS	0.045	0.538	0.025
Span thermal hysteresis (–30…+20°C), %FS	0.042	0.063	0.018
Span thermal hysteresis (+20…+60°C), %FS	0.017	0.040	0.012
Output change after pressure overload, %FS	0.006	0.006	0.004
Output change under static pressure, %FS	0.069	0.072	0.072
Long-term instability of offset, %FS	0.007	0.008	0.002
Long-term instability of pressure sensitivity, %FS	0.004	0.006	0.003
Number of samples	20	28	1200

Comparison is made under assumption that piezoresistors in both PDA-NFL and TM chip have similar doping level, sheet resistance and depth of p-n junction ($N_S = 6 \cdot 10^{18}$ cm^{-3}, $R_S = 200$ Ohm/cm^2, $x_j = 2.2$ μm) and that Wheatstone bridge formed by piezoresistors having resistance of R = 4.0 kOhm. Temperature dependence of zero output signal shows that sensitivity / span starts to change above +60 °C and BJTs enters saturation regime at T > 90 °C so PDA-NFL circuits has the upper temperature limit +60 °C. The lower temperature limit -30 °C is determined by measuring equipment.

3. Conclusion

Key parameters of pressure sensor utilizing PDA-NFL circuit based on V-NPN or L-PNP transistors are identified and analyzed. These parameters are determined by fabrication process, required stress sensitivity, solutions used

for stabilization of circuit parameters over temperature range, microstructure design, voltage supply and required common mode level for output signal.

Comparison of pressure sensitivity of the circuits with transistors sensitive / non-sensitive to pressure shows that placing transistors on the diaphragm and using them as stress-sensitive components can increase pressure sensitivity only by about 1.5 %. However, placing transistors on the diaphragm leads to much more complex circuit layout. Therefore, placing BJTs on diaphragm and making them stress-sensitive is not recommended. The theoretical model was confirmed by experiment. The possibility of significant increase in pressure sensitivity of pressure sensor with PDA-NFL circuit with respect to TM pressure sensing chip has been demonstrated. The model shows that PDA-NFL circuit utilizing V-NPN transistors has higher pressure sensitivity S, lower noise and lower temperature dependence of offset TCZ. Experimental data (or theoretical date) of pressure sensitivity of sensor chip using PDA-NFL circuit based on V-NPN and L-PNP transistors is 3.6 times (3.5 times) and 2.4 times (2.9 times) higher, correspondingly, compared to sensitivity of traditional pressure sensor chip utilizing Wheatstone bridge circuit. Sensor chip using PDA-NFL circuit based on V-NPN has lower noise than circuit based on L-PNP. However, output signal noise of PDA-NFL circuit on V-NPN is higher than output signal noise of TM sensor. In case of ASIC-assisted signal conditioning, somewhat higher output signal noise of sensor chip may be not critical. PDA-NFL circuit based on V-NPN transistors also has more than 20 times better temperature stability of offset TCZ compared to PDA-NFL circuit using L-PNP transistors by model: $TCZ_{V\text{-}NPN}$ = 0.026 %FS/°C and $TCZ_{L\text{-}PNP}$ = 0.584 %FS/°C. But experimental date was demonstrated better values: $TCZ_{V\text{-}NPN(-30\ldots+20)}$ = 0.007 %FS/°C, $TCZ_{V\text{-}NPN(+20\ldots+60)}$ = 0.010 %FS/°C and $TCZ_{L\text{-}PNP(-30\ldots+20)}$ = 0.051 %FS/°C, $TCZ_{L\text{-}PNP(+20\ldots+60)}$ = 0.056 %FS/°C. Sensor chip using PDA-NFL circuit based on V-NPN still has 2-3 times higher temperature errors than that of TM sensor chip excluding TCS. Pressure nonlinearity, pressure overload and static pressure errors are close to parameters of similar pressure sensor chips TM.

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