Average modeling of fly-buck converter

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Abstract—This document presents an average macro model for the fly-buck converter. The model can be used for both large and small signal modeling. Parasitic and lossy components are included in the model, and it is partially based on a conventional average switch model for a buck stage. For isolated output, the analytic solution of the average current in a secondary winding is proposed. The presented model is implemented in SPICE, and simulation results are compared to switching model simulation and experimental data.

I. INTRODUCTION

The fly-buck converter has become popular because it has several advantages, such as good cross regulation, line transient response, and low EMI, [1], [2]. It has a simple design and provides multiple isolated outputs. A small-signal analytical model for an ideal fly-buck converter was presented in [3], but the effects of component parasitics could not be predicted.

The proposed model can be used for both large and small signal analysis and can be simulated in time or frequency domains. The difficulty of developing such a model is that leakage inductance current has a pulsed shape and cannot be approximated with conventional small ripple approximation, [4]. To overcome this issue, the current is calculated during the instantaneous switching period, and small ripple approximation is used for the transformer’s magnetizing inductance current and capacitor voltages. The model accounts for the losses and parasitics of semiconductors and magnetic and has been implemented as a SPICE subcircuit. The following assumptions were considered: the model covers two isolated outputs, and the dead-time effect is negligible.

II. MODEL DERIVATION

The fly-buck converter’s basic structure is shown in Fig. 1. The MOSFETs Q1 and Q2 have on-state resistances $R_{on1}$ and $R_{on2}$, respectively. The transformer $T_1$ has secondary side-related leakage inductance $L_s$, magnetizing inductance $L_m$, primary winding resistance $R_{pri}$, secondary winding resistance $R_s$, and turns ratio $1:n$. The diode D1 is modeled with on-state resistance $R_D$ and forward bias voltage $V_D$. Components listed above are internal parts of the proposed model. The input voltage $v_{in}(t)$, output voltages $v_{out1}(t)$ and $v_{out2}(t)$, and the corresponding load networks $(R_1/C_1$ and $R_2/C_2$) are connected externally to the model. The converter has switching frequency $F_{sw} = 1/T$.

The main waveforms are shown in Fig. 2. The switching period is divided into three parts, and the first interval $d_1$ is the time when leakage inductance $L_s$ resets. The switch Q1 is on, and the Q2 is off. The diode D1 is forward-biased. The second interval $d_2$ is the time when the diode D1 blocks, Q1 is on, and Q2 is off. The third interval $d_3$ is the time when Q1 is off, Q2 is on, and D1 conducts. The duty cycle is determined as $d = d_1 + d_2$ and $1 - d = d_3$.

States of the converter at each time interval $d_1 - d_3$ are presented in Fig. 3. Using the small ripple approximation average, voltage across the inductor can be obtained:

$$L_m \frac{d(i_L(t))_T}{dt} = \langle v_{in}(t) \rangle_T d - \langle v_{out1}(t) \rangle_T \langle i_L(t) \rangle_T (R_{on1} d + R_{on2} (1 - d) + R_{pri}) + \langle i_{out2(d_1)}(t) \rangle_T (R_{on1} + R_{pri}) n + \langle i_{out2(d_3)}(t) \rangle_T (R_{on2} + R_{pri}) n,$$  

(1)

where $\langle x(t) \rangle_T$ represents the average value of $x$ over the switching period $T$. The currents $i_{out2(d_1)}(t)$ and $i_{out2(d_3)}(t)$ are artificially shown in Fig. 2 separately, so $i_{out2(t)} = i_{out2(d_1)}(t) + i_{out2(d_3)}(t)$ due to $i_{out2(d_2)}(t) = 0$. The average values of these currents will be obtained later.

By using the charge balance approach, the average currents for $C_1$ and $C_2$ can be found:

$$C_1 \frac{d\langle v_{out1}(t) \rangle_T}{dt} = - \langle i_{out2} \rangle_T n - \langle v_{out1}(t) \rangle_T / R_1 + \langle i_L(t) \rangle_T,$$  

(2)

$$C_2 \frac{d\langle v_{out2}(t) \rangle_T}{dt} = - \langle v_{out2}(t) \rangle_T / R_2 + \langle i_{out2}(t) \rangle_T$$  

(3)
The input voltage source’s average current can be obtained as follows:

\[
\langle i_{in}(t) \rangle_T = \langle i_L(t) \rangle_T - \langle i_{out2d1}(t) \rangle_T n \quad \text{(4)}
\]

To build the final model, the average currents \( \langle i_{out2d3}(t) \rangle_T \) and \( \langle i_{out2d4}(t) \rangle_T \) must be obtained. It can be seen from Fig. 2 that current \( i_{out2d3}(t) \) is an exponential process of magnetizing leakage inductance \( L_s \). Fig. 3c can be used to find an analytical solution for the \( \langle i_{out2d3}(t) \rangle_T \) average current. The transient process during one switching period is considered. Variables \( i_L(t) \), \( v_{out1}(t) \) and \( v_{out2}(t) \) can be replaced with constant sources for one switching period due to the small ripple approximation. The initial current in the \( L_s \) inductor is zero, so a solution for the peak and average currents can be found:

\[
\max(i_{out2}) = \frac{E_{d3}(t) F_{sw} L_s}{R_{d3} n} \left( 1 - e^{-\frac{n^2 t_{off}}{R_{d3} L_s}} \right)
\]

\[
\langle i_{out2d3}(t) \rangle_T = \frac{E_{d3}(t) F_{sw} L_s}{R_{d3} n} \left( \frac{L_s (1 - e^{-\frac{n^2 t_{off}}{R_{d3} L_s}})}{R_{d3} n^2} + t_{off} \right),
\]

where \( R_{d3} = R_{on2} + R_{pri} + (R_s + R_D) / n^2 \), \( t_{off} = (1-d) / F_{sw} \) and

\[
E_{d3}(t) = \langle v_{out1}(t) \rangle + \langle i_L(t) \rangle (R_{on2} + R_{pri}) - \frac{(\langle v_{out2}(t) \rangle + V_D)}{n}.
\]

A similar approach can be used to find \( \langle i_{out2d1}(t) \rangle_T \)’s average current during the \( d_1 \) interval. Fig. 3a represents an equivalent circuit for this interval. Transient process of the leakage inductance reset is also considered in one particular switching period. The initial current in the \( L_s \) inductor is \( \max(i_{out2}) \), found from (5), and then it resets to zero current. Thus, the solution is obtained as follows:

\[
\langle i_{out2d1}(t) \rangle_T = \frac{E_{d3}(t) F_{sw} L_s}{n^2 R_{d1} R_{d3}} \left( 1 - e^{-\frac{n^2 t_{off} R_{d3}}{R_{d1} L_s}} \right) + \frac{E_{d1}(t) F_{sw} L_s}{n^2 R_{d1}^2} \ln \left( 1 - \frac{E_{d3}(t) R_{d3}}{E_{d1}(t) R_{d1}} \left( 1 - e^{-\frac{n^2 t_{off} R_{d3}}{R_{d1} L_s}} \right) \right),
\]

where \( E_{d1}(t) = E_{d3}(t) - (v_{in}(t)) - (i_L(t)) (R_{on2} - R_{on1}) \), \( R_{d1} = R_{on1} + R_{pri} + (R_s + R_D) / n^2 \). Using (1)–(3), the schematic of the fly-buck converter model can be constructed as shown in Fig. 4. The \( \langle i_{out2d1}(t) \rangle_T \) and \( \langle i_{out2d3}(t) \rangle_T \) currents ((6) and (7)) and realization of (3) are implemented by the Gd1 and Gd2 arbitrarily behavior current sources. The E3 source, along with L1, realizes (1). The G3 source is responsible for (4), while the G4 source implements (2). The ideal diodes D1 and

**Fig. 2.** Waveforms of the fly-buck converter.

**Fig. 3.** Equivalent circuits of the converter for different time intervals.
D2 improve the convergence of the model by blocking negative voltages on the second output.

The model has next pins to connect to external circuits: node ‘Vin’ — input voltage, node ‘Vout’ — first output (non-isolated), node ‘Vout2’ — second output (isolated) and node ‘d’ — duty cycle control input (0.0...1.0 range). The reference isolated, node ‘Vout2’ — second output (isolated) and node

The parameters for simulation and testing were $V_D=1.8$ V, $R_p=10$ mOhm, and $n=5$. The external circuit contained the input cable’s 40 uH inductance, and capacitance at the input was 7.92 mF (25 mOhm ESR), $R_1=100$ kOhm, $C_1=940$ uF (35 mOhm ESR), $R_2=75$ Ohm, $C_2=2.35$ uF and the input voltage $v_{in}=50$ V. The circuit for simulation and measurement is shown in Fig. 6. The simulation results are presented in Fig. 7 and Fig. 8.

The proposed model was simulated and compared to switching modeling, along with prototype measurement. The parameters for simulation and testing were $V_D=1.8$ V, $R_{on}=0.2$ Ohm (C3D06060A two in series), $R_{on1}=R_{on2}=12$ mOhm (IPB117N20NFD), $f_{sw}=100$ kHz, $L_s=7.5$ uH, $R_s=0.07$ Ohm, $L_m=3.8$ uH, $R_{pri}=10$ mOhm, and $n=5$. The external circuit contained the input cable’s 40 uH inductance, and capacitance at the input was 7.92 mF (25 mOhm ESR), $R_1=100$ kOhm, $C_1=940$ uF (35 mOhm ESR), $R_2=75$ Ohm, $C_2=2.35$ uF and the input voltage $v_{in}=50$ V. The circuit for simulation and measurement is shown in Fig. 6. The simulation results are presented in Fig. 7 and Fig. 8.
The setup for testing is shown in Fig. 9. The measurement results are presented in Fig. 10.

Fig. 9. Fly-buck converter test setup.

Fig. 10. Measurement results. The $v_{out2}$ step response on the duty cycle changed from 0.4 to 0.5.

IV. CONCLUSION

The proposed model can be simulated for large and small signal modeling in time or frequency domains. The model accounts for parasitics of semiconductors and magnetics so losses and precise behavior can be predicted. A listing of the SPICE model was presented and it can be used for the static and dynamic behavior analysis of the fly-buck converter.

REFERENCES


