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Minimization of Transistors Count and Power in an Embedded System using GDI Technique : A realization with digital circuits

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Abstract. Gate Diffusion Input (GDI) is an advanced technique for low power digital IC design in an embedded system. This technique can be used to reduce power consumption, delay and number of transistors compared to convectional CMOS design. The standard CMOS and several different techniques for circuit design is compared with GDI technique.

Keywords: CMOS, Gate Diffusion Input (GDI), Pass Transistor Logic (PTL) etc.

1 Introduction

With the efforts for low power, high speed embedded systems the VLSI technology has scaled down to nano regimes, allowing to increase the density of the of chip i.e, more functionality to be integrated on a single chip. These efforts led to several different design techniques apart from traditional CMOS design style, GDI is one such technique.

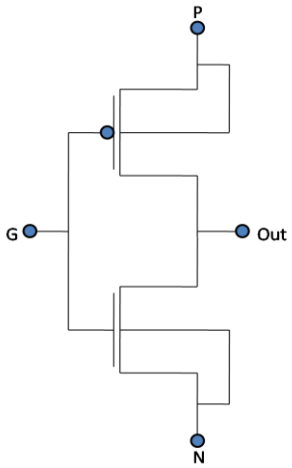
The Pass Transistor Logic (PTL) is most popular for low power digital design [7]. The advantage of PTL over standard CMOS process is: 1) high speed 2) low power dissipation and 3) lower interconnect effect due to small area. But the implementation has two basic draw backs: 1) slow operation due to reduced power supply, 2) the high input voltage level at regenerative inverter is not Vdd, the PMOS device in the

inverter is not fully turned OFF and hence direct path static power dissipation is significant.

GDI is a technique which is suitable for design of fast, low power circuits using reduced number of transistors compared to traditional CMOS design and existing PTL techniques. The aim of this work is to compare the GDI technique with other techniques; the results are compared with respect to traditional CMOS design style

2 Basic GDI Cell

The originally proposed GDI [5] is as shown in Fig. 1, which can be implemented using twin-well CMOS or SOI technology. The Fig. 2 shows the GDI cell that is compatible with standard CMOS process [1]. Some modifications in the standard CMOS inverter derives the basic GDI cell, where the sources of NMOS and PMOS are fed by input signals. GDI cell consists of 3 input terminals G, P and N.



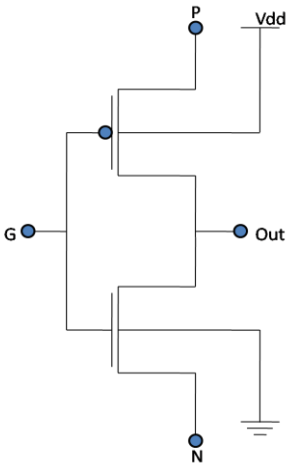


Fig. 1. originally proposed **Fig. 2.** compatible with standard CMOS process

Since it is not possible to implement all the functions of GDI, shown in Table I. Fig. 1 was proposed to implement in twin well CMOS or SOI technologies. It was believed that the bulk of both NMOS and PMOS should be connected to their source

to minimize the body effect. The bulks of NMOS and PMOS are constantly connected to GND and Vdd respectively for GDI to be implemented in standard CMOS process. The influence of body effect is similar to originally proposed GDI. With the technology scaling the impact of transistor body effect on transistor threshold is highly reduced, making less relevant in the 65nm process and below [1].

Table 1 below shows the various functions that can be implemented using basic GDI cell and the number transistors required for standard CMOS process.

Table 1. Functions implemented using GDI cell and the transistors required using standard CMOS process

N	P	G	Out	Function	No. Transistors required using GDI	No. Transistors required using CMOS
0	1	A	A`	Inverter	2	2
0	B	A	A`B	Function1	2	6
B	1	A	A`+B	Function2	2	6
1	B	A	A+B	OR	2	6
B	0	A	AB	AND	2	6
C	B	A	A`B+AC	MUX	2	12
B`	B	A	A`B+B`A	XOR	4	16
B	B`	A	AB+A`B`	XNOR	4	16

3 Operation Analysis of GDI Cell

Low swing of output signals is the problem in the PTL technique due to threshold drop across the single channel pass transistor, additional buffering circuitry is required to avoid this problem. To understand the analysis of low output swings in GDI consider the analysis of Function1. Table III shows the set of logic states and

functionality of Function1.As we know that PMOS provides strong 1 and week 0 at its output and NMOS provides strong 0 and week 1 at its output From Table 2 it can be seen that low swing of output occurs when A=0, B=0, in this case the output is threshold voltage of PMOS ($V_{Tp)}$. This for the transition of B=1 to B=0 when A=0. When B=1 the GDI operates as a regular inverter, which is widely used as a digital buffer for logic level restoration without the swing drop from previous stage

Table 2. Input Logic States, Functionality and Swing of Function 1

A	B	Functionality	Output
0	0	PMOS Transmission Gate	V_{Tp}
0	1	CMOS Inverter	1
1	0	NMOS Transmission Gate	0
1	1	CMOS Inverter	0

4 Comparison with Other Logic Styles

4.1 Basic GDI Functions

The circuits were tested in a 0.35-µm twin well CMOS process at 3.3v, 40MHz at 27 ^{degree} C [3, 5]. The comparisons were carried out for the GDI, standard CMOS, transmission gate and NMOS pass gate. For faith full comparisons of different techniques, comparisons are carried out from cells in series with buffers. GDI and transmission gate test setup has two basic cells followed by on one output buffer while the NMOS pass gate contains two buffers one after the other while the standard CMOS requires no buffers. Among all, the GDI requires minimum number of transistors. The average power consumed with reference to CMOS is listed in Table 3 below. Table 4 shows the implementation of logic gates using GDI and standard CMOS logic to show transistor required.

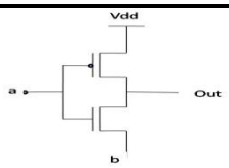
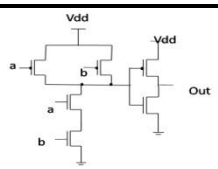
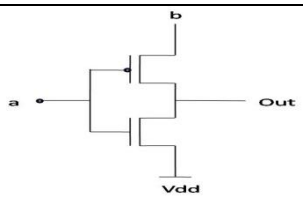
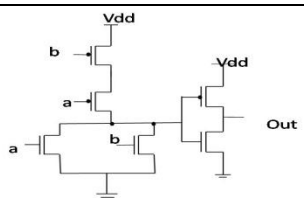
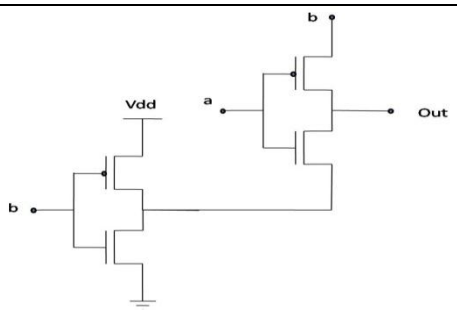
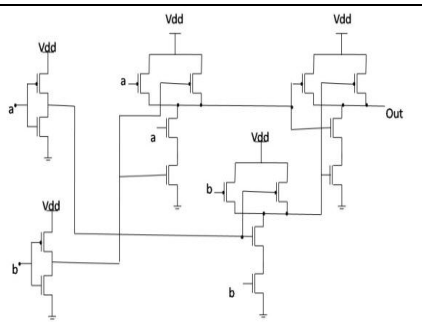
Table 3. Percentage of Power consumed by GDI, TG, N-PG with respect to CMOS

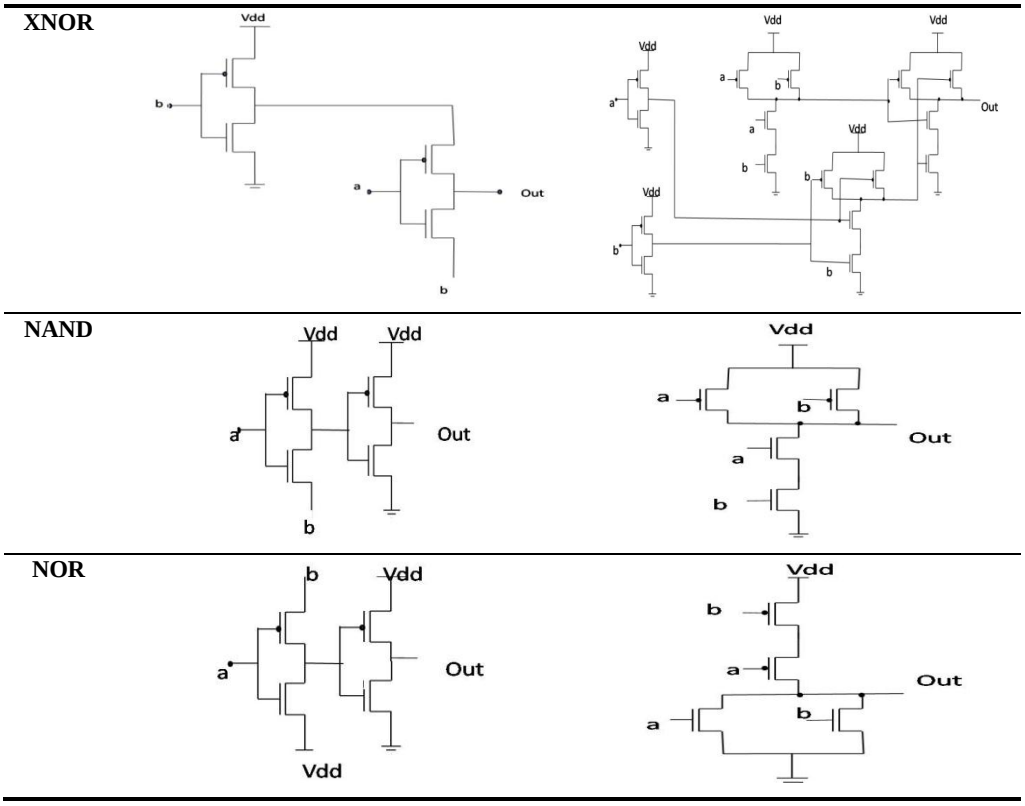
	GDI	TG	N-PG
MUX	71.8	90.3	95.5
OR	79.9	110	99.08
AND	75.3	90.3	88.26
Function 1	69	70.35	70.35
Function 2	74.2	77	68.67

From Table 3 it can be seen that GDI technique consumes least percentage of power compared to CMOS and transmission gate logic and NMOS pass gate logic.

Low swing of output signals

Table 4. Implementation of Logic gates using GDI technique and Standard CMOS

	GDI	CMOS
AND		
OR		
XOR		



4.2 8-Bit Comparator

The 8-bit Comparator is implemented using 1.6µm CMOS process [4]. The comparison is carried for GDI technique, Standard CMOS process and NMOS pass gate. It is seen that GDI provides the best performance among the all, as it can be seen in Table 5, all 3 circuits are implemented 96 transistors.

4.3 4-Bit Multiplier

The multiplier is implemented using 0.5µm CMOS technology with 3.3V supply voltage [4]. Comparison results are shown in Table 6. 26 transistors are used in GDI technique while 44 Transistors are used in standard CMOS.

Table 5. Comparison of GDI, CMOS and N-PG 8-Bit Comparator

Logic Style	CMOS	GDI	N-PG
Power (mW)	1.82	1.41	3.87
Number of Transistors	96	96	96

Table 6. Comparision of GDI and CMOS 4-Bit Multiplier

Logic Style	CMOS	GDI
Power (mW)	1.265	0.3079
Number of Transistors	44	26

4.4 Adder

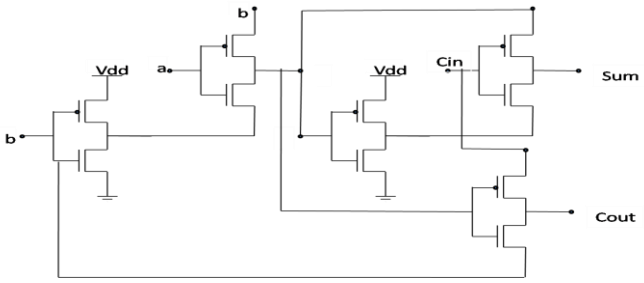


Fig. 3. Implementation of Full Adder using GDI

GDI full adder circuit is shown above in fig 3, it requires only 10 transistors where 26 transistors are required using static CMOS process. In the worst case Sum has 4-T delay while Cout has 3-T delay. However, it has a benefit of low power consumption as it uses GDI cell

4.5 D-Flip Flop

Fig.4 shows the D-Flip Flop implementation using GDI. It is based on master slave connections of two GDI D-Latches. Each Latch consists of four basic GDI cells. To implement D Flip Flop it requires total of 18 transistors (16 shown in Fig.4 plus 2 transistors for D`). The circuit was implemented using 0.35µm and 0.18µm at 3.3 V and 1.8V respectively and its consumed 812.7uW and 151.7uW respectively [3].

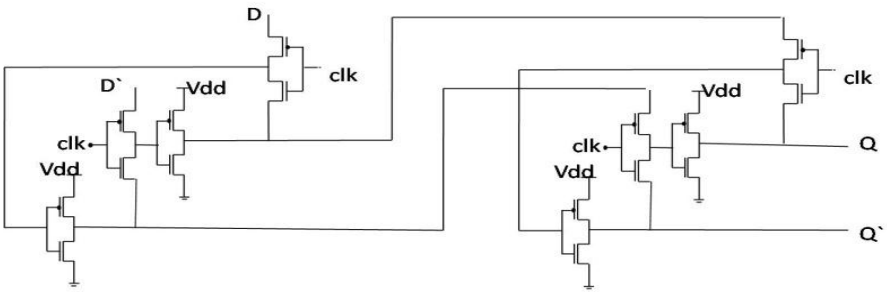


Fig. 4 D-Flip Flop Implementation using GDI

5 Simulation and Results

Basic GDI Functions have been simulated using SPICE and the simulated outputs are show in Fig.4 below. These are the outputs of Basic GDI Cell without employing any level restoring circuits at their outputs. It can be seen that the outputs are within the range of noise margin to predict the correct output of the logic implemented by the Basic GDI cell. The simulation results of few functions as listed in Table I are shown in Fig. 5(a) to Fig. 5(d)

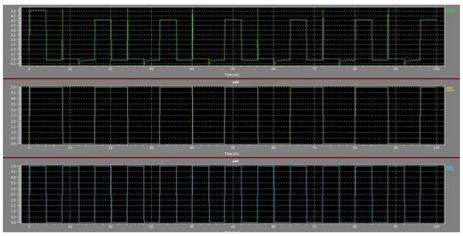


Fig. 5(a). Output of GDI AND Gate

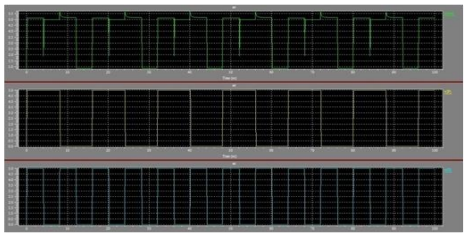


Fig. 5(b). Output of GDI OR Gate

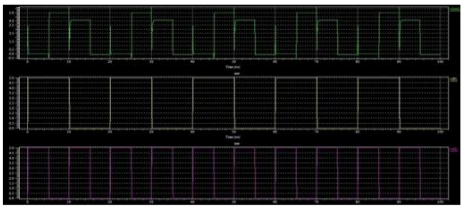


Fig. 5(c). Output of GDI XOR Gate

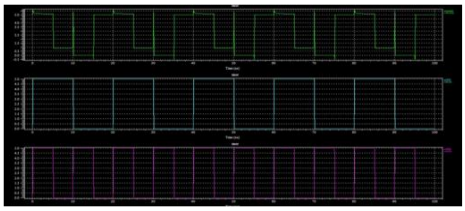


Fig. 5(d). Output of GDI XNOR Gate

6 Discussion

The simulated results confirm the functionality of all logical function as spitted in Table I. Power consumption as well as space reduction are among few major achievements in this new technique. The problem of threshold drop can be reduced by the proper sizing of transistors or by using level restoring circuits. The system may find its wide application in Embedded system ICs used in industrial as well as domestic applications.

7 Conclusion

GDI technique is implemented for Basic Logic Gates and some Digital circuits. Comparisons are made among GDI, standard CMOS and some pass transistor logics. The analysis shows that the GDI technique is novel and an effective technique for reducing power consumption and the Transistor count which will effectively reduce the size of the chip. GDI will allow high density of Fabrication as now a day's chip area is very important parameter. With respect to chip area, power consumption and transistor count, GDI technique is significantly advantageous over other technique

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