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Dissertation on

'Double Input Boost/Y-Source DC-DC Converter for

Renewable Energy Sources'

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under the guidance of

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING MASTER OF TECHNOLOGY



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MASTER OF TECHNOLOGY

CERTIFICATE

This is to certify that the Dissertation entitled

'Double Input Boost/Y-Source DC-DC Converter for Renewable Energy

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is a bonafide work carried out by

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In partial fulfilment for the completion of Final Year course work in the Program of Study M.Tech in Electrical and Electronics Engineering (Power Electronic Drives and Energy Systems) under rules and regulations of PES University, Bengaluru during the period Aug. 2018 – May 2019. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report. The dissertation has been approved as it satisfies the 4th semester academic requirements in respect of project work.

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DECLARATION

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ABSTRACT

With the increasing adoption of renewable energy sources by domestic users, decentralisation of the grid is fast becoming a reality. Distributed generation is an important part of a decentralised grid. This approach employs several small-scale technologies to produce electrical energy close to the end users or consumers. The higher reliability of these systems proves to be of advantage when compared to traditional generation systems. Multi-Input Converters (MICs) perform a decisive function in Distributed Energy Resources (DERs). Making use of such MICs prove to be beneficial in terms of size, cost, number of components used, efficiency and reliability as compared to using several independent converters. This thesis proposes a double input DC-DC converter which makes use of a quasi Y-source converter in tandem with a boost converter. The quasi Y-source converter has the advantage of having a very high gain for low duty cycles. The associated operating modes are analysed and the operation of the MIC is verified using simulation result. A hardware prototype is built for large signal analysis in open loop. Different loads are applied and the efficiency of the MIC as a whole as well as the load sharing between the different sources is investigated.

Keywords: *DC-DC Converter*, *Y-Source Impedance Network*, *Distributed Generation*, *Multi-Input Converters*

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CHAPTER 1

Introduction

1.1 Introduction

Multi-Input Converters (MICs) are growing in popularity because of their newfound applications in the modern energy system. The entry of renewables into the energy system is a precursor to the rapid spread of distributed generation technologies. Renewable energy sources like solar and fuel cells are DC in nature. Also, the ability of renewable sources to be installed on a small scale is leading to the adoption of these power sources at the domestic level. Distributed generation at domestic level which includes significant amounts of renewable energy sources is one of the most important applications of power electronics based converters. To aggregate the numerous sources, the development of a Multi-Input converter takes prominence.

In most modern day systems, the power generated, output load demand or sometimes both change dynamically and are not the same at any given instant as they ideally should be. Providing a perfect synergy between the input power source and the output sink is thus, a complicated task. Additional sources thus become necessary to aid the primary power source in satisfying the load demand in a reliable manner.

It is in such situations that MICs have started to play a pivotal role. One single MIC can thus be able to replace numerous converters leading to significant savings. These converters can interface different input voltage levels, and blend their individual superiorities to feed the load. MICs are able to perform this task with a reduced number of components while also simultaneously aiming for higher reliability and efficiency.

The usual approach to connecting numerous diverse sources is to connect them in either series or in parallel. However, the sources that are connected in parallel must carry the same current, which is not always feasible. Since the sources may have varying voltage levels, connecting them in parallel directly will not be feasible. This is where MICs come into play. The MICs consists of different power electronic converters which convert the different input voltages to into a single output voltage which can supply the load.

A prime example of such a system with multiple sources is a Photo Voltaic (PV) system which is shown in Fig 1.1. This generic system consists of two power sources, the PV cells and the battery pack. The supply by the solar cells are not consistent and depends on uncontrollable factors like availability of clear skies and the time of the day. This system requires additional supplies like a battery pack or ultra-capacitors to handle the excess load demand. In case of excess generation of energy by the solar cells because of clear sunny days, the use of bidirectional converters enable the batteries to be recharged. The use of multiple converters is therefore very common in a large system having multiple photovoltaic sources.



Fig. 1.1 Multiple photovoltaic sources employing Multi-Input Converters

Hybrid Electric Vehicles (HEVs) are another system which makes use of multiple converters. HEVs use an internal combustion engine along with a battery pack or ultracapacitors which can act either as a power source or as an energy storage unit depending on various conditions. Use of such a system enables the internal combustion engine to run at optimum efficiency and any additional energy requirement during acceleration or for power steering can be supplied by the connected batteries or ultracapacitors. Using more than one electric power source in such a system improves the efficiency of the system. Thus the use of multiple converters become inevitable. The block diagram of such a system having two bidirectional converters is shown in Fig 1.2.



Fig. 1.2 Hybrid Electric Vehicles with multiple converters

In systems such as these, it becomes beneficial to use a single Multi-Input Converter instead of several discrete converters as it uses a lesser number of components, has more stability, is simpler to control and also helps to reduce losses. The block diagram of a system using Multi-Input Converters is shown in Fig 1.3.



Fig. 1.3 Photovoltaic system employing Multi-Input Converters

1.2 Types of Multi-Input Converters

Based on the topology of connection of the multiple converters, the Multi-Input Converter can be classified as parallel or series connected MIC. Fig 1.4 shows a series connected Multi-Input Converter system which is usually used for low power wind and solar systems. This converter layout is derived by connecting the output stages of the

two DC-DC converters in series.



Fig. 1.4 Series Multi Input Converter

However, output voltage and current regulation are very difficult in such a configuration as both the sources in question may be of a dynamic nature. The main disadvantage of this system is that the load current flows through both the converters. This causes a high power loss. The gating signals for the individual converters are conjunctive in nature which may lead to circulating currents between the two input sources.

Fig 1.5 shows a representative diagram of a system which uses several individual converters connected in parallel to form a single Multi-Input Converter. All the converters are linked together at the DC bus. An important feature of such a system is that all the converters are controlled independently. Such a system is however inherently complex and expensive because of multiple conversion stages and communication devices which are required for each of the conversion stages.



Fig. 1.5 Parallel Multi Input Converter

1.3 Thesis organisation

The thesis is organised as follows. Chapter II contains the literature referenced for this thesis. Chapter III contains descriptions about the circuits that make up the proposed converter. It also contains a brief about the proposed converter and its modes of operation. A summary of the method used to determine a closed loop operation is also given. Chapter IV contains the procedure and the results of the simulation performed in MATLAB-Simulink. Chapter V contains the design procedure of the components used in building the hardware of the converter. It also contains the pictures of the output which was obtained by the hardware. Chapter VI contains the analysis of various results obtained and also the scope for improvement of this converter in the future.

CHAPTER 2

Literature Review

Multi-Input Converters (MICs) are growing in popularity because of their newfound applications in the modern energy system which includes significant amounts of renewable energy sources and distributed generation [1]. The pressure to increase the share of renewable energy in the existing energy infrastructure and to remove the dependence of oil is driving the adoption of renewable sources like solar, wind, and fuel cells[2]. Renewable energy sources are primarily DC in nature. Another feature of renewable sources is the absence of large generating areas. Household adoption of renewable energy creates a large network of distributed generation sources[3]. Distributed Generation is set to change the way electric power systems operate according to [4]. The electric power generation trends point towards the disbursed generators of size kW to MW sitting at the loads as opposed to traditional centralized generators sized from 100MW to GW and are located at far of places where natural resources are more readily available. In most modern day systems, the generation and demand balance is dynamic and difficult to maintain without complicated demand side management techniques [5]. Maintaining the balance between the input source and the output sink is thus, a complicated task. Additional sources thus become necessary to aid the primary source to satisfy the load demand.

Liu and Chen have given the general systematic approach to synthesize Multi-Input Converters in [6]. The Quasi Y-source converter and the boost converter act like a Pulsating Current Source Cell according to [6] and hence they must be added together in parallel before being supplied to the load. Various types of double input converters which draw from two sources either simultaneously or individually have been implemented in [7], [8] and [9].

Various types of Multiple Input Converter topologies have been compared in [10].

These converters occupy less space, use fewer semiconductors thereby reducing the manufacturing cost. Zhao and Kwasinki propose a multiple input converter in [11] especially for distributed generation applications which allows for the integration of various renewable sources into a common DC bus. A Multi-Input topology with two separate boost and buck-boost input legs have been developed in [12] that aims to enhance the availability of distributed generation sources in microgrids. The multiple input converter is arranged in modules which contain the common parts and the different input sources are arranged in submodules. This is a highly flexible and scalable topology that is suitable for renewable energy sources. A further extension of this is the development of multi-port converters with bidirectional power flow capability which finds increasing use as the developments in storage technology continue to grow. These multi-port converters have been investigated in [13], [14] and [15] among others. These applications find mention in the development of stand-alone hybrid microgrids with battery storage capabilities.

The Y-source impedance network is introduced in converters in order to achieve higher voltage gains even with small duty cycles. A single switch DC-DC boost converter which makes use of this impedance network has been implemented in [16]. These types of impedance networks make use of a tightly coupled transformer to achieve the high gains observed. The quasi Y-Source DC-DC converter proposed in [17] is a modification to the Y-source converter. This modification over the Y-source converter enjoys continuous input current characteristics thus enabling it to be used in fuel cells and photovoltaic systems. Coupled inductors have been used in literature [18] to create magnetically coupled impedance sources in converters to create high gain at small duty cycles. The Quasi Y-source converter belongs to this class of converters. The DC-DC Boost Converter [19] is one of the most elemental power electronics converters which are used to boost the DC voltage.

A family of different DC-DC boost converters are defined in [20] which makes use of the high voltage gain applications of this topology in various places like photovoltaic cells and fuel cells. The Y-source impedance network is combined with boost modules to provide high gain, continuous input current and inrush current suppression. The thermal performance and the efficiency of the Y-source converter have been investigated in [21]. Major losses like conduction, switching, core and winding losses, and capacitor ESR losses have been evaluated for different gains and winding factors. The results show that higher is the voltage gain and the winding factor, higher is the power loss and junction temperature. Various experimental prototypes of the Y-source converter have been built in [22] which need a small duty ratio to obtain high voltage gains. The Y-source converter belong to a class of impedance source DC-DC converters which have been deduced for high gain conversions in [23], [24], [25] and [26].

Double Input Converters have been developed in [27] and energy from two diverse sources with different I-V characteristics have been integrated to feed a load in a single stage. Different control strategies and power management techniques have been explored. [28] develops a double input converter for renewable or non-renewable sources and then increases the number of inputs and achieves a higher efficiency for this operation. Low output voltage ripple is achieved even with the addition of multiple sources. Gummi, Karteek and Ferdowsi have investigated the use of a double input converter in electrical drives for electric vehicles in [29]. Applications for these types of converters which make use of multiple numbers of input power sources are on the rise. The reduced number of parts in such systems are proving to be of advantage. [29] also tries to develop a systematic approach to developing a Multi-Input converter for such hybrid systems.

CHAPTER 3

Multi-Input Converter

3.1 Synthesis of Multi-Input Converter

According to [6], the rules for synthesis of MIC depends upon the type of the converters being used in the system. Both the Quasi Y-Source Converter and the Boost Converter represent a Pulsating Current Source Cell (PCSC) when the voltage sink is removed. The Quasi Y-Source Converter is considered as a PWM converter. The converter represents a pulsating current source with a diode in series. To develop a Multi-Input Converter, the PCSC has to be connected in parallel with one of the branches of the Quasi Y-Source Converter. These converters are not connected in series because the current which is flowing through the connected branch of the boost converter will be clamped by the pulsating current source. The series diode in the boost converter blocks any voltage differences which may crop up between the voltage imposed on the boost converter.

When the PCSC of the boost converter is being introduced to the voltage sink portion of the Quasi Y-Source converter, it is connected across the voltage sink with its outgoing current terminal tied to the positive terminal of the output sink.

The following sections give more detail about the topology of the modified Y-Source converter which is one of the converters used while synthesizing this particular Multi-Input Converter.

3.2 Quasi Y-Source Converter

The quasi Y-Source DC-DC converter proposed in [17] a modification to the Y source converter which uses a high impedance network. This modification enjoys continuous input current characteristics enabling it to be used in fuel cells and photovoltaic systems. The high voltage gain is also an added advantage.

Coupled inductors are finding their way into power electronics circuits[18]. One important application of coupled inductors is in creating magnetically coupled impedance networks. These impedance networks were used in synthesising the Z - Source Inverter in 2003. These Z - Source converters initially had a very low voltage gain. With improvements and modifications, several new topologies have been developed based on the impedance networks. The Y source Converter is one among them. Other notable topologies include the quasi Z - Source and the τ - Source networks.

The presence of an input diode in the above-mentioned networks means the converters which make use of these networks inherently suffer from discontinuous input current. Continuous input current is an important necessity when the converter is used for renewable energy sources like fuel cells or photovoltaic cells. Especially in photovoltaic systems, drawing continuous input current helps the system to operate more accurately around the maximum power point. The improvement in the efficiency of the PV system is especially noticeable when continuous current is drawn[17]. The chopping of the current experienced when discontinuous current is drawn is known to negatively affect the lifetime of the PV cells. To achieve a continuous input current when using magnetically coupled impedance sources, a large filter inductor and capacitor were added to the original network [17] resulting in a Quasi Y Source Converter. The Y-Source impedance network is capable of achieving very high gain in smaller duty cycles.



Fig. 3.1 Circuit Diagram of Quasi Y-Source DC-DC Converter

The circuit of the Quasi Y Source Converter is shown in Fig 3.1. By using KVL, we

 $(1-6d_{st})^{-1}$

can find the mesh equations during shoot through and non shoot through cycles. The output equation for the Quasi Y Source Converter is given as,

$$v_o = \frac{1}{1 - \frac{N_1 + N_2}{N_2 - N_3}} V_{in} = \frac{V_m}{1 - \delta D_{ST}}.$$
(3.1)

Where,
$$\delta = \frac{N_1 + N_2}{N_2 - N_3} > 1$$
 and, $B = \frac{1}{1 - \delta d_{st}}$

As seen in the above equations, the boosting gain depends on the winding ratios of the three windings (N1, N2, and N3) and the duty ratio of the switch used. By manipulating the winding ratios, a high gain can be achieved for a relatively lower duty ratio. For the same duty cycle, a significantly larger gain is achieved than a Z source converter or a boost converter. The gain of the Quasi Y-Source DC-DC Converter for different winding factors δ , and turns ratio (N1:N2:N3) is calculated from Eq. 3.1 and shown in Table 3.1:

NI:N2:N3	δ	Gain
(1:3:1),(1:5:2),(2:4:1)	2	$(1 - 2d_{st})^{-1}$
(1:2:1),(3:3:1),(2:4:2)	3	$(1 - 3d_{st})^{-1}$
(2:2:1),(1:3:2),(5:3:1)	4	$(1 - 4d_{st})^{-1}$
$(1\cdot 4\cdot 3)(2\cdot 3\cdot 2)(3\cdot 2\cdot 1)$	5	$(1 5d)^{-1}$

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Table 3.1 Gain of Quasi Y-Source Converter for different δ and turns ratios

3.3 Zeigler Nichols Tuning Method

(2:4:3), (3:3:2), (4:2:1)

The Zeigler-Nichols tuning method is a popular algorithm which is used to tune PID controllers. This is a heuristic approach, designed to sufficiently reach an immediate goal without any guarantees that the result found is the most optimal solution that can be found. The four important parameters that can be controlled using the PID controller are rise time, overshoot, settling time and the steady-state overshoot. Rise time is defined as the time taken for the plant to rise to 90% of the desired level for the first time. Rise time is an important measure of the responsiveness of the system. This usually depends on the stray capacitances and inductances in the circuit. The overshoot refers to how much the peak level is higher than the steady state whereas settling time is the time it takes for the system to converge to steady state. Overshoot is useful for the stability of

the system and to look after the constraints of the components in the system. Overshoot is calculated only in the transition period. The settling time is also important for the stability of the system. The steady state error is the difference between the steady state output and the desired output. Steady state error gives the accuracy of the system. The effects of each of the controller parameters K_p , K_i and K_d can be summarized as in Table 3.2.

Response	Rise Time	Overshoot	Settling Time	Steady State Error
K_p	Decreases	Increases	No Change	Decreases
K_i	Decreases	Increases	Increases	Eliminated
K_d	No Change	Decreases	Decreases	No Change

Table 3.2 PID Controller parameters and their effect on system response

Table 3.2 gives an assessment of the effect of the various controller parameters on the system response. By fine-tuning the controller parameters we can arrive at a sufficiently good enough model. However, to find the starting point for the tuning is a cumbersome process. This is where the Zeigler Nichols Method comes into play. Zeigler and Nichols conducted a large number of experiments. They then proposed these rules for determining the controller parameters, namely, K_p , K_i and K_d which are arrived on the basis of the transient response of the plant. They many methods, but in this thesis, only one method is explored. This is the Zeigler Nichols second tuning method. In this method, the tuning is first started with a proportional controller to a closed loop system as shown in Fig 3.2.



Fig. 3.2 Closed Loop Control System with Proportional Controller

The tuning is then begun with a very low or zero value of K_p and marked up gradually. This is done until a steady state oscillation is seen. The gain which is obtained is noted as K_{cr} , or ultimate gain. The period of this sustained oscillation is noted down as P_{cr} , or ultimate period as shown in Fig 3.3.



Fig. 3.3 Sustained Oscillation observed during Zeigler Nichols Tuning

Based on the arrived ultimate gain and ultimate period, and by referring to the gain estimator chart given by Zeigler and Nichols, the controller parameters are chosen. The gain estimator chart is given in Table 3.3.

Controller	K_p	K_i	K_d
P Controller	$0.5K_{cr}$	∞	0
PI Controller	$0.45K_{cr}$	$\frac{1}{1.2}P_{cr}$	0
PID Controller	$0.6K_{cr}$	$0.5P_{cr}$	$0.125P_{cr}$

Table 3.3 Gain Estimator Chart

3.4 Double Input Converter

The proposed Multi-Input Converter topology is derived from two discrete converters: a Boost DC-DC converter and the Quasi Y-Source Converter. In this type of converter, both the inputs can be used to supply the load either individually or simultaneously is the case demanded by the load. The proposed system is illustrated in Fig 3.4.



Fig. 3.4 Proposed Double Input DC-DC Converter

The boost converter consists of a Pulsating Source Current cell which can be connected parallel to the loaded sink in order to synthesise a Multi-Input Converter. This strategy is utilised in this topology. V_{in1} , V_{in2} and V_o are the two input voltages and the output voltage of the converter. N_1, N_2 and N_3 are the number of winding turns of the coupled inductor. The voltage across the primary of the coupled inductor is given by v_L . V_{C1} and V_{C2} are the voltages seen across the capacitors C_1 and C_2 . The voltages across the input inductors and are given by V_{l1} and V_{l2} . This converter draws power from the two discrete sources simultaneously as well as individually. Since there are two switches, S1 and S2, there are four modes of operation as illustrated in Fig 3.5.

The four modes of operation are as follows:

- Mode I: S1 off, S2 on. The equivalent circuit for this mode is shown in Fig 3.5
 (a). The load is supplied by the quasi Y-Source converter, while the input inductor of the boost converter is getting charged.
- Mode II: S1 on, S2 off. Fig 3.5 (b) shows the equivalent circuit for this mode of operation The load is entirely supplied by the boost converter while the input



Fig. 3.5 Operating Modes in the Double Input Converter

inductor of the quasi Y-Source Converter gets charged.

- Mode III: S1 off, S2 off. Fig 3.5(c) shows the equivalent circuit for this mode of operation. In this mode of operation, both the boost converter as well as the quasi Y-Source Converter supplies the load.
- Mode IV: S1 on, S2 on. Fig 3.5 (d) shows the equivalent circuit for this mode of operation. In this mode of operation, the load is disconnected from the supply. The input inductors of both the boost converter as well as the quasi Y Source Converter gets charged during this period.

A control strategy can be adapted to chose which of the two sources should be used a the primary power source. One of the sources can be used to supply the base load while the other can compensate for changes in load, or change in the source supply. The simulation of this converter is shown in the next chapter along with the associated results.

CHAPTER 4

Simulation

4.1 Simulation Parameters

MATLAB is a numerical computing environment which allows matrix manipulations and plotting of functions and implementations of algorithms. Simulink is an extension to the MATLAB environment which allows for a graphical programming environment. Modelling, simulating and analyzing of many multidomain components is possible through Simulink. MATLAB-Simulink was used to simulate the Multi-Input Converter in order to verify its performance. The parameters of the simulation blocks are given in Table 4.1.

Description	Values
Input Voltage (v_{in1})	12V
Input Voltage (v_{in2})	24V
Desired Output Voltage (v_o)	48V
Power	80-120W
Input Inductors (L_1 and L_2)	1mH
DC Blocking Capacitor (C_1)	$470\mu F$
DC Blocking Capacitor (C_2)	$150\mu F$
Output Capacitor (C_o)	$470\mu F$
Turns Ratio of Transformer	3:2:1
Switching Frequency	20kHz

 Table 4.1 Simulation parameters for the Double Input Converter

4.1.1 Turns ratio of Three Winding Transformer

The turns ratio is selected based on the data from Table 3.1 in order to obtain a gain factor of 4. The duty cycles are controlled in such a manner that the boost converter converts 30V to 40V and the quasi Y source converter converts 10V to 40V. The block diagram created for simulation in MATLAB-Simulink is represented in Fig 4.1.



Fig. 4.1 Simulation Block Diagram

4.1.2 Zeigler Nichols Tuning

Zeigler Nichols Second Tuning Method has been used for estimating the controller parameters for the PI controller to be implemented. With K_i and K_d kept at zero, K_p was increased until consistent oscillations were observed in the output. This value is known as the ultimate gain. The period of oscillation thus found was 5ms.

Ultimate gain = 1.3 Ultimate period = 5ms From the Table 3.3, $K_p = 0.675$ $K_i = 162$

The corresponding controller loop which is designed using Zeigler Nichols tuning method is shown in Fig 4.2.

4.2 Simulation Results

The output voltage of 48V is shown in Fig 4.3 and the gating signals are shown in Fig 4.4. The fact that the Quasi Y-Source converter requires a very small duty cycle to achieve high gain can be observed through this simulation.

The boost converter requires a duty cycle of 50% to boost the input voltage from 24V to 48V whereas the Quasi Y-Source achieves even greater gain for noticeably smaller duty cycles.



Fig. 4.2 Control Loop



Fig. 4.3 Output Voltage of the Double Input Converter



Fig. 4.4 Gating signals for the MOSFETs in the Double Input Converter

CHAPTER 5

Hardware Implementation

5.1 Hardware Design

The hardware of the proposed double input converter has been implemented with an open loop control system. The gating signals are generated by Pulse Width Modulation (PWM) using TL494 ICs. A gate is then added in order to amplify the low power signal from the microcontroller or the controller IC which is the TL494 in this case and generate a high current drive input to the gate of the semiconductor switch, which is a MOSFET in this case. The converter is built as per the circuit diagram. Toroidal cores are chosen for the input inductors. A three winding transformer is wound as per the required ratio in order to give high input impedance to the Quasi Y -Source converter. The design and selection of components are covered in the following subsections.

5.1.1 PWM Generation

The TL494 IC is used for the generation of gating pulses using Pulse Width Modulation (PWM). The TL494 consists of the complete PWM power control circuitry on a single chip. However, since two synchronized pulses are required for the open loop control, two TL494 ICs are used in a master-slave configuration. Synchronizing multiple oscillators in a common system is conveniently achievable due to the flexible architecture of the TL494. The internal oscillator in the TL494 is used only for the generation of a saw-tooth waveform on the timing waveform. This can be to constrain the oscillator on the slaves by maintaining a compatible saw-tooth waveform externally to the timer capacitor terminal. Terminating the R_T terminal to the reference supply will constrain the internal oscillator of the slave TL494.

The two TL494s used are synchronized by establishing one IC as the master. The oscillator of this IC is programmed normally. The oscillators of the slave ICs are dis-

abled as explained above. The saw-tooth waveform created by the master is used as the modulating signal for the slave IC by tying all the C_T pins together as shown in Fig 5.1.



Fig. 5.1 Master-Slave configuration in TL494

5.1.2 Gate Driver

The gate driver functions like a power amplifier that takes in low power inputs from the controller ICs or microcontrollers and delivers a high current drive for driving the gate of power semiconductor switches like power MOSFETs. A gate driver is used when the PWM controller cannot provide sufficient output current which is required to drive the gate capacitance of the MOSFET. The gate drive function is partitioned off from the PWM controller in order to restrain the controller from heating and be more stable. This is because of the high peak currents which are required to drive a power MOSFET at high frequencies but cause high heat dissipation are eliminated from the controller IC.

The Gate Driver circuit designed in this project has three major components: a buffer, an optocoupler and a gate driver IC.

5.1.2.1 Buffer Amplifier

The buffer circuit prevents the loading of the source. If the load to a voltage source is a low value, it practically shorts the source and draws too much current from the source for which the source is not rated which is harmful to the source. So by cascading a buffer after a source provides a division of labour- the source only generated the correct voltage and the buffer provides the demanded current keeping the voltage constant AND without loading the source as the buffer has very high input impedance, it draws negligible current from the original source, thereby preventing loading. The buffer also prevents unintended current division (i.e, basically provides the required amount of cur-

rent to all the load impedance). In a nutshell, wherever there is a possibility of loading of source, buffers are used. A CD4050B opamp based buffer is used for this purpose. The schematic of the buffer circuit used is shown in Fig 5.2.



Fig. 5.2 A Schematic of Buffer Amplifier

5.1.2.2 Optocoupler

The Optocoupler is used to provide electrical isolation between the high voltage power converter section and the low voltage controller section of the circuit. It protects the sensitive, low voltage components and isolates them on a PCB. The 6N136 IC is used as the optocoupler in this driver circuit. This IC allows for the transmission of an electrical signal between two electrically isolated circuits. It consists of two parts: an LED that emits infrared light and a photosensitive transistor that detects the light from this LED and is driven whenever the LED is switched ON. Optocouplers are used in circuits which are susceptible to voltage surges, lightning strikes, power supply surges etc in order to protect the low voltage controllers. The optocoupler can effectively remove electrical noise from signals and thereby allow the use of small digital signals to control larger AC voltages. The schematic of the optocoupler used is shown in Fig 5.3.

Calculation of suitable resistance for the optocoupler circuit design is done using the forward current of 6N136 from the datasheet. According to the datasheet, the 6N136



Fig. 5.3 Schematic of Optocoupler

has a forward current of 16mA with a forward voltage of 1.9V.

5V - 1.9V = 3.1V has to developed across the resistance R_1 .

Therefore,
$$R_1 = \frac{3.1V}{16mA} = 193.7 \ ohm.$$

To saturate the phototransistor and to develop a value of 0V at the output, R_2 must develop 12V when passing a current of 16mA (assuming 115% CTR value).

$$R_2 = \frac{12V}{16mA} = 750 \ ohm$$

A value of 750 ohm is thus used.

5.1.2.3 Gate Driver

A gate driver is then used to accept low power control signals from a controller and amplify it into a larger current output which drives the power MOSFET. IR2101 is a high and low side driver which is used for driving the power MOSFETs used in the converter. The IR2101 driver is capable of a high voltage and high-speed operation. It is capable of driving a power MOSFET with it's independent high and low side referenced output channels. It includes a floating channel which is used for the bootstrap operation

for driving high side switches. This is not used in this project as both the switches in this topology are low side switches. A range of voltages from 10V to 20V can be used to supply the gate. This IC is 3.3V, 5V and 15V logic input compatible. A gate-source resistance is then added before giving the gate drive to the gate of the MOSFET. This gate is usually used in high-frequency operations. Usually, this resistance is provided to prevent accidental turn on due to noise or other factors like gate-to-drain internal capacitance (Miller's capacitance). The schematic of the IR2101 gate driver is shown in Fig 5.4.



Fig. 5.4 A Schematic of IR2101 Gate Driver

5.1.3 Inductor Design

Two input inductors are used in the design of this converter. Both have an inductance of 1mH, however, the current carried by each inductor is different.

5.1.3.1 Input Inductor for Quasi Y-Source Converter

Inductance = 1 mH

Maximum current = 2.85A

Energy stored in inductor,

$$E = 0.5LI^2 = 0.046125J \tag{5.1}$$

Area Product for the core,

$$A_p = A_w A_c = \frac{2E_L}{K_w K_c J B_m} = 18050 mm^4$$
(5.2)

A core with a high resistivity is picked to reduce the eddy current losses. A Ferrite core is chosen for this purpose. T45 core is selected for calculations. The number of turns is given by,

$$N = \frac{LI_m}{A_c B_m} = 123 \tag{5.3}$$

The cross section of the winding is given by,

$$a_w = \frac{I}{J} = \frac{2.85}{3 * 10^6} = 9.5E - 7 \tag{5.4}$$

Wire Gauge of SW18 is chosen.

Upon performing the cross check to see if the wires can be accommodated in the window area, it fails. The window area is not enough to accommodate the windings. By choosing a different core, (O42813TC), the calculations are performed again. From the new core, the number of turns is are,

$$N = \frac{NI_m}{2.301 * 0.25} = 18 \tag{5.5}$$

This new core will be able to accommodate the new windings satisfactorily.

5.1.3.2 Input Inductor for Boost Converter

Inductance = 1mH Maximum current = 0.75A

Energy stored in inductor,

$$E = 0.5LI^2 = 0.000281J \tag{5.6}$$

Area Product for the core,

$$A_p = A_w A_c = \frac{2E_L}{K_w K_c J B_m} = 0.125 * 10^{-8} m^4$$
(5.7)

A core with high resistivity is selected to minimize the eddy current losses. A Ferrite core is chosen for this purpose. A O41206TC core is selected for calculations. The number of turns is given by,

$$N = \frac{LI_m}{A_c B_m} = 14 \tag{5.8}$$

The cross section of the winding is given by,

$$a_w = \frac{I}{J} = \frac{0.75}{3 * 10^6} = 2.5E - 7 \tag{5.9}$$

Wire Gauge of SW23 is chosen. The window area is sufficient to accommodate the windings and passes the cross check.

5.1.4 Switch Selection

IRFZ34 Power MOSFET has been chosen as the switch for this converter. This MOS-FET has a V_{ds} of 60V which is suitable for the voltage ratings selected for this converter. Combined with a fast switching and a low on-resistance (R_{ds}) of 0.01 ohm for a V_{gs} of 10V, this switch is a cost-effective option.

5.2 Hardware Results

Since the main application of this converter is in distributed generation, two separate sources are required. For this purpose 12V, lead-acid batteries are used. The source to the Quasi Y-Source Converter is a 12V supply and a single battery is used as input. For the boost converter, for which the input is 24V, two batteries are connected in series. Both the inputs are connected to the converter. The PWM pulses which are finally obtained from the gate driver is given as input to the MOSFET gate. The required duty cycles are tuned beforehand.



Fig. 5.5 Hardware Implementation of the Double Input Converter

The eventual hardware implementation of the Double Input Converter is shown in Fig 5.5.

The output of 48V can be achieved by connecting the Quasi Y-Source Converter and the Boost converter independently.

Both the Quasi Y-Source Converter as well as the Boost Converter are now supplied with 12V and 24V respectively. The output of 48V is observed as shown in Fig 5.6.



Fig. 5.6 Operation of Double Input Converter

Care must be exercised while tuning the duty cycles as the boost converter is an inherently unstable converter, especially when operated in an open loop. High duty cycles will exponentially increase the gain to very high voltage levels and this may

cross the voltage ratings of the components in the converter leading to malfunction.

The analysis of the results obtained by operating the converter under different loads has been presented in the next chapter.

CHAPTER 6

Results and Conclusion

6.1 Results

A Multi-Input Converter which is arrived at by a combination of a boost converter and a Quasi Y-source converter has been proposed in this thesis. This dual input converter has some useful features like continuous input current, ability to run either individually or simultaneously and also has a very high boost ability. The proposed control loop which has been derived using Zeigler Nichols estimation has been able to satisfactorily operate for the given voltage and power ratings. These features enable this converter to be applied for renewable energy sources. The results have been confirmed by simulation using MATLAB-Simulink. A working hardware prototype which has open loop control



Fig. 6.1 Input power vs Output load

has been built to validate the circuit topology. Output loads in the range of 3W to

25W have been used as a sink to the circuit and various parameters have been recorded. Fig 6.1 shows the trend of input power required to supply the given output load. It also shows the input power drawn by the two converters in order to supply the given load.

In the case of converters with multiple sources, most sources will not share the load equally. One of the sources will always try to supply an excessive fraction of the load. Typically, this is the source with the highest power rating. It will always try to deliver the highest current possible according to the design. The voltage will drop as it supplies more current and when the voltage has dropped to the point where it is lower than the next source, the other source will be activated. In a system with multiple sources, all the sources may contribute towards fulfilling the load, but the proportion is widely unequal. In the absence of any control strategy, the load sharing is highly dependent on the voltages of the different sources used.



Fig. 6.2 Load Sharing by the two converters

This graph shows the pattern of load sharing by the two converters when different loads are applied. The efficiency of the converter is extremely low at small loads. The boost converter supplies the majority of the load in this converter in the open loop configuration. In the absence of any control strategy which dictates which source is to be the primary source, most of the current is hence drawn by the boost converter. This is because two 12V batteries are connected in series to derive the 24V input for the boost converter. Hence the strain on the battery is lower and this source can supply greater

current than a single 12V battery. Fig 6.2 shows the sharing of load between the two converters at different values of loads.

Fig 6.2 shows that the boost converter which has 2 batteries supplies the majority of the load as the output load is increased. This is a potential problem because if one of the converters fails, then the other converter will go from supplying a percentage of the load to supplying the full load. During this time the voltage will droop in the absence of a closed loop control system. The transient will be even more severe if the converter which is supplying a higher percentage of the load fails.

Fig 6.3 shows the plot of efficiency against output power. The efficiency of the double input converter increases when it is loaded closer to the rated values. At very low loads, the efficiency is very poor.



Fig. 6.3 Efficiency of the Double Input Converter at different loads

At very low loads, the efficiency is very poor. This can be explained by the conduction losses and the V-I overlap losses which are usually seen in DC-DC Converters at low loads. V-I overlap losses are proportional to the input voltage, load current and switching frequency and occur due to the V-I overlap region that is seen in converters with rapid switching cycles. But at low loads, the conduction losses which are caused due to current ripples dominate the overlap losses as the power dissipated due to current ripples remain same whereas the overlap losses reduce due to low load currents. Under light loads, the gate drive losses which occur due to the charging and discharging the gate capacitance dominate the load.

Thus, a DC-DC converter with multiple input ports can be successfully implemented to supply a common load. The load will be shared by the different sources depending on their capacities.

6.2 Conclusion

With the increasing adoption of renewable energy in the power grid, it has become imperative to look for unique and efficient converter designs. Renewable energy sources are primarily DC in nature. It is also one of the leading types of distributed generation. In these conditions, the development of a Multi-Input Converter to aggregate all the different distributed sources and feed a common load assumes importance. This project proposes such a converter which can take in two different sources of different voltage levels, aggregate their power and feed a load. The use of different topologies of converters in this aggregated converter has been well demonstrated. A Quasi Y-Source converter which can give a high gain is used for this converter. A boost converter has also been used to demonstrate the use of multiple converters. With this converter, the load can be shared between the two sources. The use of multiple converters has been eliminated. This method of using a multiple input converter to aggregate different power sources can be used as a viable method to integrate renewables into the existing power infrastructure.

6.3 Future Scope

To create a Multi-Input Converter for distributed generation sources for real-life applications, the open loop version will not be satisfactory. A control strategy has to developed where one source is chosen to be the primary source and supplies the bulk of the load while the other source acts as an auxiliary source kicking in at peak demands. The converter must be able to handle dynamic loads as well as dynamic sources as is the case with most of the renewable sources. Current sharing strategies must be developed so that both the converters supply a pre-determined share of the load. This is essential so that both the converters age at the same rate and replacement will be easier.

An interesting method of current sharing will be to choose one converter as the master. This master converter will be employed with intelligent driver controls and will supply the base load. The slave controller will boost the voltage to meet the dynamic power requirements.

The performance of the converter with different types of distributed generation sources like solar, wind, biomass, fuel cells etc must be evaluated. Primary sources must be selected based on the power availability. Auxiliary sources must be used to supply the peak load demand. Adding extra redundant converters to the existing topology can ensure reliability. Conducting reliability studies of such converters and developing redundancy indices will be an area of research.

Another upcoming area of research will be to develop bidirectional converters which allow the integration of storage devices as well. Advances in storage technology, as well as the availability of cheap second-hand batteries disposed of EV's, will increase the use of batteries as a part of the power grid. Higher power production from renewables will be used to store the batteries which will then be used during peak loads. Having bidirectional multi-port converters will be useful in such conditions.

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Appendices

Appendix A

DATASHEETS

- CD4050B Datasheet
- TL494 Datasheet
- 6N135 Datasheet
- IR2101 Datasheet



Sample 8

🖥 Buy



CD4049UB, CD4050B

E Design

Reference

SCHS046J-AUGUST 1998-REVISED SEPTEMBER 2016

CD4049UB and CD4050B CMOS Hex Inverting Buffer and Converter

Technical

Documents

Features

- CD4049UB Inverting
- CD4050B Noninverting
- High Sink Current for Driving 2 TTL Loads
- High-to-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1 µA at 18 V Over Full Package Temperature Range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V Parametric Ratings .

2 Applications

- CMOS to DTL or TTL Hex Converters
- CMOS Current Sink or Source Drivers
- CMOS High-to-Low Logic Level Converters

3 Description

Tools &

Software

The CD4049UB and CD4050B devices are inverting and noninverting hex buffers, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logiclevel conversions. These devices are intended for use as CMOS to DTL or TTL converters and can drive directly two DTL or TTL loads. (V_{CC} = 5 V, $V_{OL} \le 0.4 \text{ V}$, and $I_{OL} \ge 3.3 \text{ mA.}$)

Support &

Community

Device	Information ⁽	1)
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PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD4049UBE, CD4050BE	PDIP (16)	3.90 mm × 19.30 mm
CD4049UBD, CD4050BD	SOIC (16)	9.90 mm × 3.91 mm
CD4049UBDW, CD4050BDW	SOIC (16)	10.30 mm × 7.50 mm
CD4049UBNS, CD4050BNS	SO (16)	19.30 mm × 6.35 mm
CD4049UBPW, CD4050BPW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic Diagram of CD4050B



Copyright © 2016, Texas Instruments Incorporated 1 of 6 Identical Units



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Schematic Diagram of CD4049UB





SCHS046J-AUGUST 1998-REVISED SEPTEMBER 2016

5 Pin Configuration and Functions



Pin Functions: CD4049UB

PIN		1/0	DESCRIPTION	
NAME	NO.	1/0	DESCRIPTION	
A	3	I	Input 1	
В	5	I	Input 2	
С	7	I	Input 3	
D	9	I	Input 4	
E	11	I	Input 5	
F	14	I	Input 6	
G	2	0	Inverting output 1. $G = \overline{A}$	
Н	4	0	Inverting output 2. H = \overline{B}	
I	6	0	Inverting output 3. I = \overline{C}	
J	10	0	Inverting output 4. J = \overline{D}	
К	12	0	Inverting output 5. $K = \overline{E}$	
L	15	0	Inverting output 6. L = \overline{F}	
NC	13, 16	—	No connection	
VCC	1	_	Power pin	
VSS	8	_	Negative supply	



Technical Documents



Support & 20 Community



TL494

SLVS074H-JANUARY 1983-REVISED MARCH 2017

TL494 Pulse-Width-Modulation Control Circuits

Features

- Complete PWM Power-Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source Current
- Output Control Selects Single-Ended or **Push-Pull Operation**
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance
- Circuit Architecture Allows Easy Synchronization

2 Applications

- **Desktop PCs**
- Microwave Ovens
- Power Supplies: AC/DC, Isolated, With PFC. > 90 W
- Server PSUs
- Solar Micro-Inverters
- Washing Machines: Low-End and High-End
- E-Bikes
- Power Supplies: AC/DC, Isolated, No PFC, < 90 W
- Power: Telecom/Server AC/DC Supplies: **Dual Controller: Analog**
- Smoke Detectors
- Solar Power Inverters

3 Description

The TL494 device incorporates all the functions required in the construction of a pulse-widthmodulation (PWM) control circuit on a single chip. Designed primarily for power-supply control, this device offers the flexibility to tailor the power-supply control circuitry to a specific application.

The TL494 device contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from -0.3 V to V_{CC} -2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can drive the common circuits in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 device provides for push-pull or singleended output operation, which can be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL494C device is characterized for operation from 0°C to 70°C. The TL494I device is characterized for operation from -40°C to 85°C.

Device Information ⁽¹⁾							
PART NUMBER	PACKAGE (PIN)	BODY SIZE					
	SOIC (16)	9.90 mm × 3.91 mm					
TI 404	PDIP (16)	19.30 mm × 6.35 mm					
12494	SOP (16)	10.30 mm × 5.30 mm					
	TSSOP (16)	5.00 mm × 4.40 mm					

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram







6 Pin Configuration and Functions



Pin Functions

PIN		TVDE	DESCRIPTION					
NAME	NO.	TIPE	DEGONFTION					
1IN+	1	I	Noninverting input to error amplifier 1					
1IN-	2	I	Inverting input to error amplifier 1					
2IN+	16	I	Noninverting input to error amplifier 2					
2IN-	15	I	Inverting input to error amplifier 2					
C1	8	0	Collector terminal of BJT output 1					
C2	11	0	Collector terminal of BJT output 2					
СТ	5	—	Capacitor terminal used to set oscillator frequency					
DTC	4	I	Dead-time control comparator input					
E1	9	0	Emitter terminal of BJT output 1					
E2	10	0	Emitter terminal of BJT output 2					
FEEDBACK	3	I	Input pin for feedback					
GND	7	_	Ground					
OUTPUT CTRL	13	I	Selects single-ended/parallel output or push-pull operation					
REF	14	0	5-V reference regulator output					
RT	6	_	Resistor terminal used to set oscillator frequency					
V _{CC}	12	_	Positive Supply					

6N135, 6N136

Vishay Semiconductors





www.vishay.com

DESCRIPTION

/ISHA

The 6N135 and 6N136 are optocouplers with a GaAlAs infrared emitting diode, optically coupled with an integrated photo detector which consists of a photo diode and a high-speed transistor in a DIP-8 plastic package.

Signals can be transmitted between two electrically separated circuits up to frequencies of 2 MHz. The potential difference between the circuits to be coupled should not exceed the maximum permissible reference voltages.

FEATURES

- Isolation test voltages: 5300 V_{RMS}
- TTL compatible
- High bit rates: 1 Mbit/s
- · High common-mode interference immunity
- Bandwidth 2 MHz
- Open-collector output
- External base wiring possible
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

AGENCY APPROVALS

- UL1577 file no. E52744, double protection
- DIN EN 60747-5-5 (VDE0884-5) available with option 1
- cUL components acceptance service no. 5A
- CQC GB8898-2011, GB4943.1-2011

ORDERING INFORMATION					
6 N 1 3 # PART NUMBER	- X 0 # #	DIP-8 Option 6 TAPE AND REEL Option 7 Option 9 > 0.7 mm			
AGENCY CERTIFIED / PACKAGE	CTR (%)				
UL, CSA	≥7	≥ 19			
	6N135	CNI10C			
DIF-0	010105	6IN 136			
DIP-8, 400 mil, option 6	-	6N136-X006			
DIP-8, 400 mil, option 6 SMD-8, option 7	- 6N135-X007T ⁽¹⁾	6N136-X006 6N136-X007T ⁽¹⁾			
DIP-8, 400 mil, option 6 SMD-8, option 7 SMD-8, option 9	- 6N135-X007T ⁽¹⁾ -	6N136-X006 6N136-X007T ⁽¹⁾ 6N136-X009T ⁽¹⁾			
DIP-8, 400 mil, option 6 SMD-8, option 7 SMD-8, option 9 VDE, UL, CSA	- 6N135-X007T ⁽¹⁾ - ≥7	6N136-X006 6N136-X007T ⁽¹⁾ 6N136-X009T ⁽¹⁾ ≥19			
DIP-8, 400 mil, option 6 SMD-8, option 7 SMD-8, option 9 VDE, UL, CSA DIP-8	- 6N135-X007T ⁽¹⁾ - ≥7 -	6N136-X006 6N136-X007T ⁽¹⁾ 6N136-X009T ⁽¹⁾ ≥ 19 6N136-X001			
DIP-8, 400 mil, option 6 SMD-8, option 7 SMD-8, option 9 VDE, UL, CSA DIP-8 SMD-8, option 7	- 6N135-X007T ⁽¹⁾ - ≥7 - 6N135-X017T ⁽¹⁾	6N136-X006 6N136-X007T ⁽¹⁾ 6N136-X009T ⁽¹⁾ ≥ 19 6N136-X001 6N136-X017T			

Note

(1) Also available in tubes; do not add T to end

Document Number: 83604

For technical questions, contact: <u>optocoupleranswers@vishay.com</u> THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT <u>www.vishay.com/doc?91000</u>









6N135, 6N136

Vishay Semiconductors

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)								
PARAMETER	CONDITION	SYMBOL	VALUE	UNIT				
INPUT								
Reverse voltage		V _R	5	V				
Forward current		١ _F	25	mA				
Peak forward current	t = 1 ms, duty cycle 50 %	I _{FSM}	50	mA				
Maximum surge forward current	t \leq 1 µs, 300 pulses/s		1	A				
Thermal resistance		R _{th}	700	K/W				
Power dissipation	T _{amb} = 70 °C	P _{diss}	45	mW				
OUTPUT								
Supply voltage		VS	-0.5 to 15	V				
Output voltage		Vo	-0.5 to 15	V				
Emitter base voltage		V _{EBO}	5	V				
Output current		Ι _Ο	8	mA				
Maximum output current			16	mA				
Base current		Ι _Β	5	mA				
Thermal resistance			300	K/W				
Power dissipation	T _{amb} = 70 °C	P _{diss}	100	mW				
COUPLER								
Storage temperature range		T _{stg}	-55 to +150	°C				
Ambient temperature range		T _{amb}	-55 to +100	S				
Soldering temperature	max. \leq 10 s, dip soldering \geq 0.5 mm from case bottom	T _{sld}	260	°C				

Note

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

ELECTRICAL CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)										
PARAMETER	TEST CONDITION PART SYMBOL			MIN.	TYP.	MAX.	UNIT			
INPUT										
Forward voltage	I _F = 16 mA		V _F	-	1.33	1.9	V			
Breakdown voltage	I _R = 10 μΑ		V _{BR}	5	-	-	V			
Reverse current	V _R = 5 V		I _R	-	0.5	10	μA			
Capacitance	$V_R = 0 V$, f = 1 MHz		Co	-	30	-	pF			
Temperature coefficient, forward voltage	I _F = 16 mA		$\Delta V_F / \Delta T_A$	-	-1.7	-	mV/°C			
OUTPUT										
Logic low supply current	I_F = 16 mA, V_O = open, V_{CC} = 15 V		I _{CCL}	-	150	-	μA			
Logic high supply current	$I_F = 0$ mA, $V_O =$ open, $V_{CC} = 15$ V		I _{CCH}	-	0.01	1	μA			
	$I_F = 16 \text{ mA}, I_O = 1.1 \text{ mA}, V_{CC} = 4.5 \text{ V}$	6N135	V _{OL}	-	0.1	0.4	V			
Output voltage, output low	I_F = 16 mA, I_O = 3.0 mA, V_{CC} = 4.5 V	6N136	V _{OL}	-	0.1	0.4	V			
Output ourrent, output high	$I_F = 0 \text{ mA}, V_O = V_{CC} = 5.5 \text{ V}$		I _{OH}	-	3	500	nA			
Output current, output high	$I_F = 0 \text{ mA}, V_O = V_{CC} = 15 \text{ V}$		I _{OH}	-	0.01	1	μA			
COUPLER										
Capacitance (input to output)	f = 1 MHz		C _{IO}	-	0.6	-	pF			

Note

• Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

International **IGR** Rectifier

Data Sheet No. PD60043 Rev.O

IR2101(S)/IR2102(S)&(PbF)

Features

- Floating channel designed for bootstrap operation Fully operational to +600V Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V, and 15V logic input compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs (IR2101) or out of phase with inputs (IR2102)
- Also available LEAD-FREE

Description

The IR2101(S)/IR2102(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL

HIGH AND LOW SIDE DRIVER

Product Summary

VOFFSET	600V max.
I _O +/-	130 mA / 270 mA
Vout	10 - 20V
t _{on/off} (typ.)	160 & 150 ns
Delay Matching	50 ns

Packages



output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



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IR2101(S)/IR2102(S) & (PbF)

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
VB	High side floating supply voltage	-0.3	625		
VS	High side floating supply offset voltage		V _B - 25	V _B + 0.3	
V _{HO}	High side floating output voltage		V _S - 0.3	V _B + 0.3	V
V _{CC}	Low side and logic fixed supply voltage		-0.3	25	v
VLO	Low side output voltage	-0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (HIN & LIN)	-0.3	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient		—	50	V/ns
PD	Package power dissipation @ $T_A \le +25^{\circ}C$	(8 lead PDIP)	—	1.0	
		(8 lead SOIC)	—	0.625	W
Rth _{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	C/ VV
ТJ	Junction temperature		_	150	
Τ _S	Storage temperature		-55	150	°C
Т	Lead temperature (soldering, 10 seconds)		_	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V _S + 10	V _S + 20	
VS	High side floating supply offset voltage	Note 1	600	
VHO	High side floating output voltage	Vs	VB	V
Vcc	Low side and logic fixed supply voltage	10	20	
VLO	Low side output voltage	0	Vcc	
VIN	Logic input voltage (HIN & LIN) (IR2101) & (HIN & LIN) (IR2102)	0	Vcc	
T _A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

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Appendix B

TOROIDAL CORE DETAILS



FERRITE TOROIDS

Ferrite Toroids

Ferrite toroids offer high magnetic efficiency as there is no air gap and the cross-sectional area is uniform. Magnetics[®]toroids are available in many sizes (outside diameters ranging from 2 mm to 140 mm) and <u>materials</u> (permeabilities ranging from 900µ to 15,000µ). Different coatings can be applied to ferrite toroids to increase winding ease and improve voltage breakdown. <u>Hardware</u>, such as toroid mounts and headers, is available.

LEARN MORE

Key Characteristics

Composition: Mn • Zn • Fe

Shapes: Toroid

Sizes: 3 mm to 140 mm

Permeability: $M=15,000\mu$, $W=10,000\mu$, $J=5,000\mu$, $T=3,000\mu$, $F=3,000\mu$, $P=2,500\mu$, $R=2,300\mu$, $L=900\mu$, $C=900\mu$

Coating Color: Grey

Typical applications for high permeability ferrite toroids, 5,000µ <u>J material</u>, 10,000µ <u>W material</u>, and 15,000µ <u>M material</u> include common mode chokes, EMI filters, broadband transformers, pulse transformers and current transformers. Special sizes of ferrite toroids are available in 5,000 <u>J material</u> for Ground Fault Interrupter (GFCI) applications. 900µ <u>L material</u>, 2,300µ <u>R material</u>, 2,500µ <u>P material</u>, and 3,000µ <u>F material</u> toroids are excellent choices for high frequency transformers.

Material Characteristics

Nine different materials for Magnetics Ferrite Toroids (**L**, **R**, **P**, **F**, **T**, **J**, **W**, **C**, **M**) exist.

VIEW MATERIALS SUMMARY

Ferrite Toroid Part Number Identification

HOW TO ORDER: MAGNETICS FERRITE CORES

	A _L nH/T ² (nominal)						L _e Path	A _e Cross	 V.						
Part #	L 900µ	R 2300µ	Ρ 2500μ	F 3000µ	J 5000µ	W 10000µ	M 15000µ	С 900µ	Length mm	Section mm ²	Volume mm ³	WaAc cm ⁴	OD mm	ID mm	Height mm
<u>8626</u>						<u>18,760</u>			215	377	81,165	91.2	85.7	55.5	25.24
<u>9715</u>		<u>3,025</u>	<u>3,464</u>		<u>6,575</u>	<u>11,178</u>			255.3	267.2	68,281	90.8	102	65.8	15
<u>9718</u>		<u>4,127</u>	<u>4,486</u>		<u>8,972</u>	<u>15,252</u>			259	370	96,000	106	107	65	18
<u>9725</u>		<u>5,732</u>	<u>6,230</u>		<u>9,346</u>	<u>21,184</u>			259.31	514.3	133,351	171	107	65	25
<u>9740</u>		<u>3,200</u>	<u>3,477</u>		<u>6,955</u>	<u>11,823</u>			381.5	422.3	161,086	372	140	106	25